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MS-7916

ATX

Ver:1.0

Intel -SharkBay plamform (Z97-XPOWER)

CPU:

Haswell-Reflash LGA1150
CPU ISL6388 12Phase

System Chipset:

Lynx Point Z97

Onboard Chip:

HD Audio Codec:ALC1150
LAN-Killer 2005
SIO:NCT6792D
Flash ROM: SPI 64 MB X2
CLK GEN: IDT6V49325
CLK BUF: 9DBV0841
USB Charge: SLG55583A

PWM:

VCORE: VRD12.5 -ISL6388 - 12Phase
DDR : UP1504S - 2Phase
PCH(1.05V) -OP+MOS

Other:

SATA3.0 x4(PCH)
SATA3.0 x2 (ASM1061 SATA 6G *1)
M.2 X1(SATA*2/PCIE*2)
REAR USB3.0 X4 (ASM1074 *1)
REAR USB3.0 X2 (PCH)
REAR USB3.1 X2(ASM1042 *1)
FRONT USB3.0 X2 (PCH)
REAR USB2.0 X2
FRONT USB2.0 X4(Super Charge *2)

Main Memory:

DDRIII (800/1066/1333/1666MHz) * 4 (Dual Channel)

ACPI:

UPI-uP7501+uP1714

Expansion Slots:

PCI Express (X16) Slot * 3

PCI Express (X1) Slot * 4

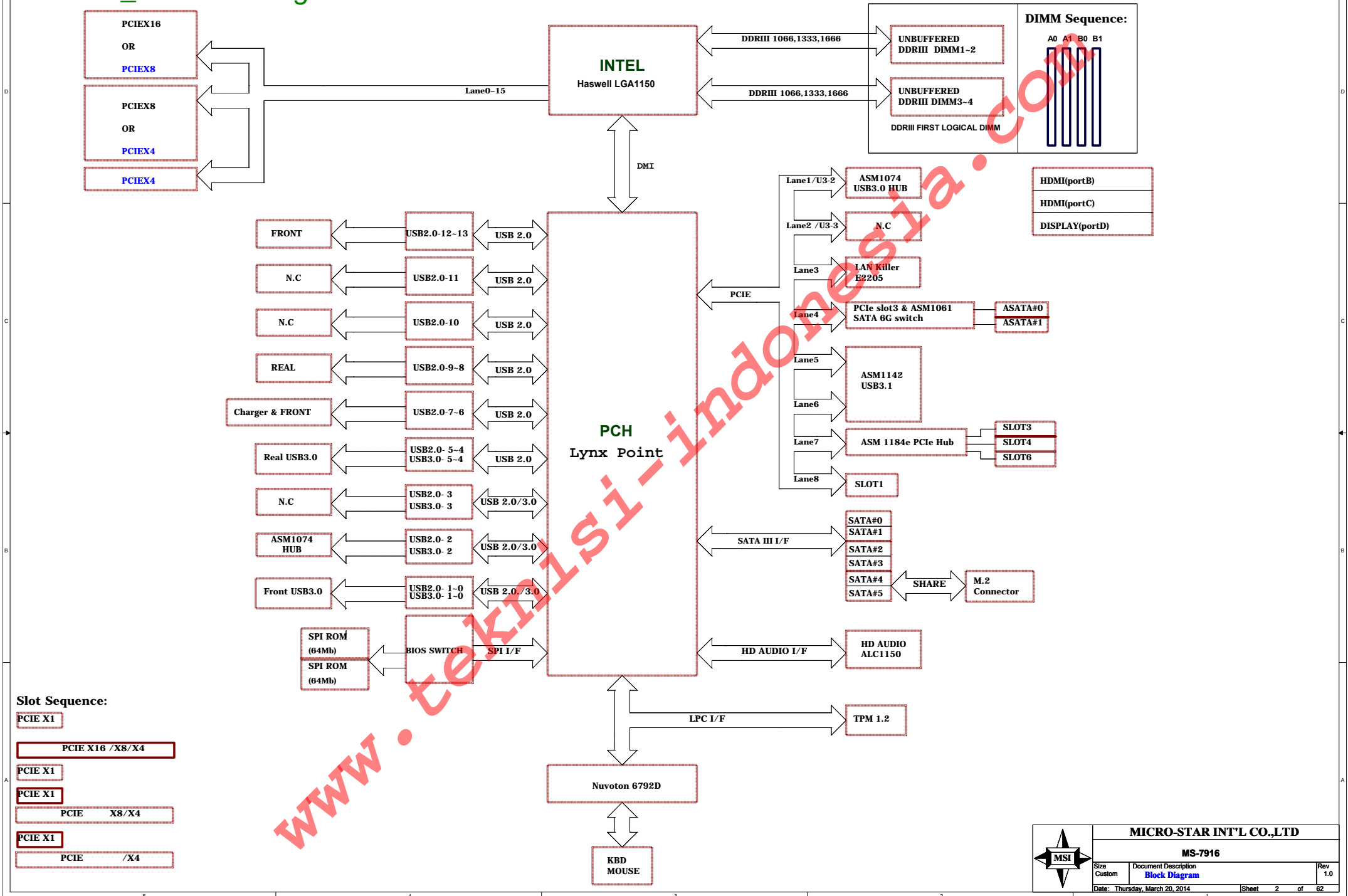


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MS-7916_0A Block Diagram





GND

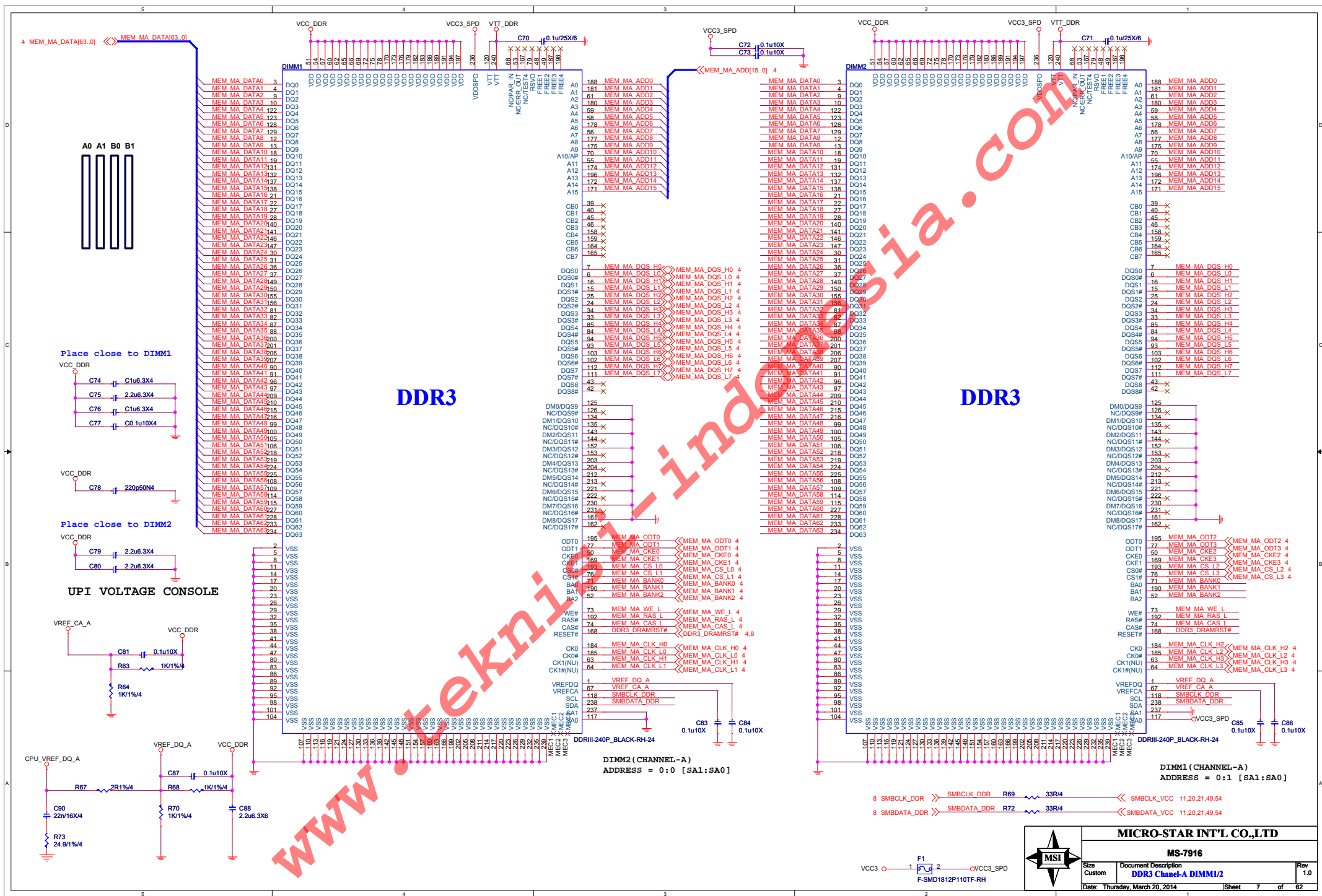
GND



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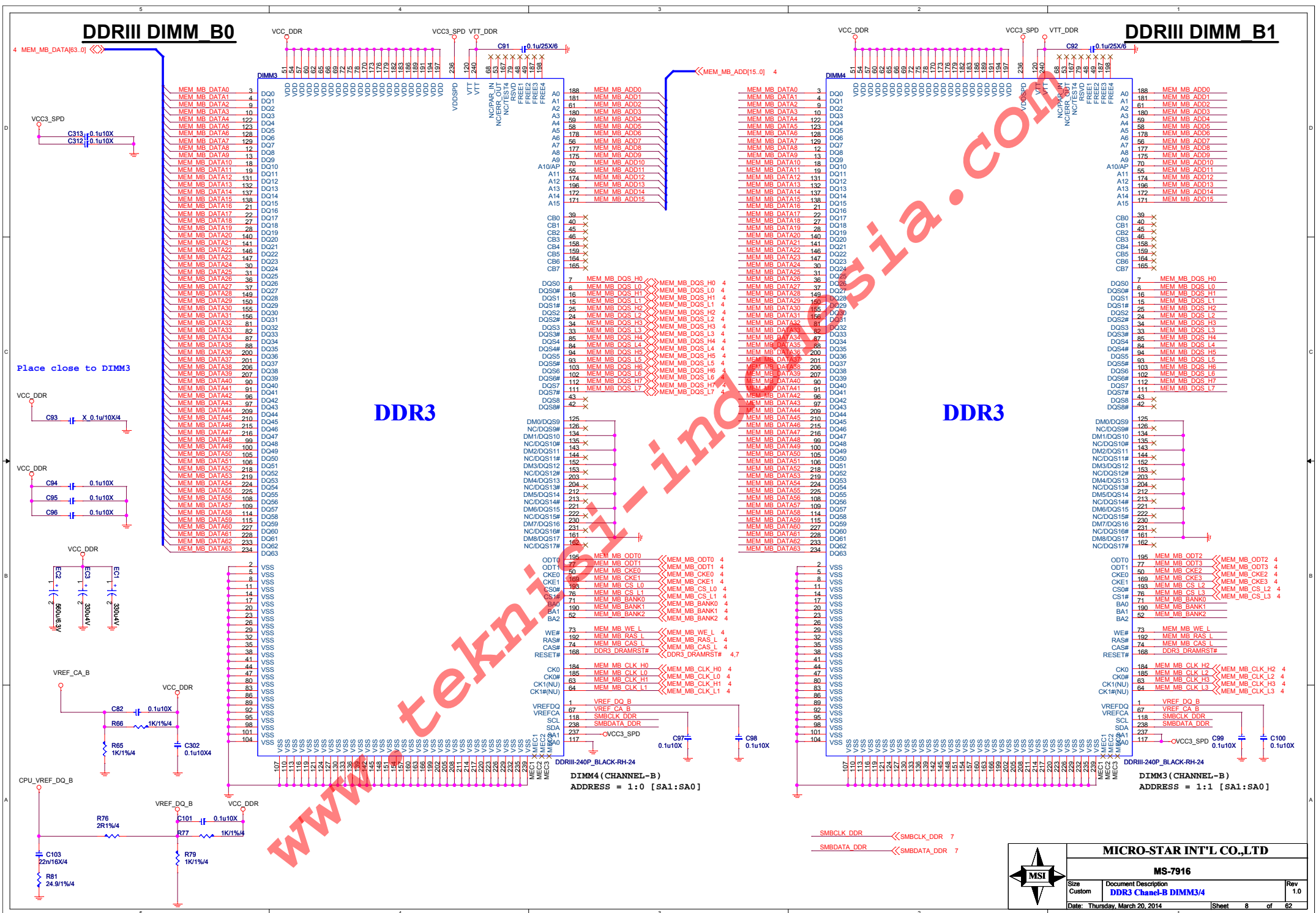


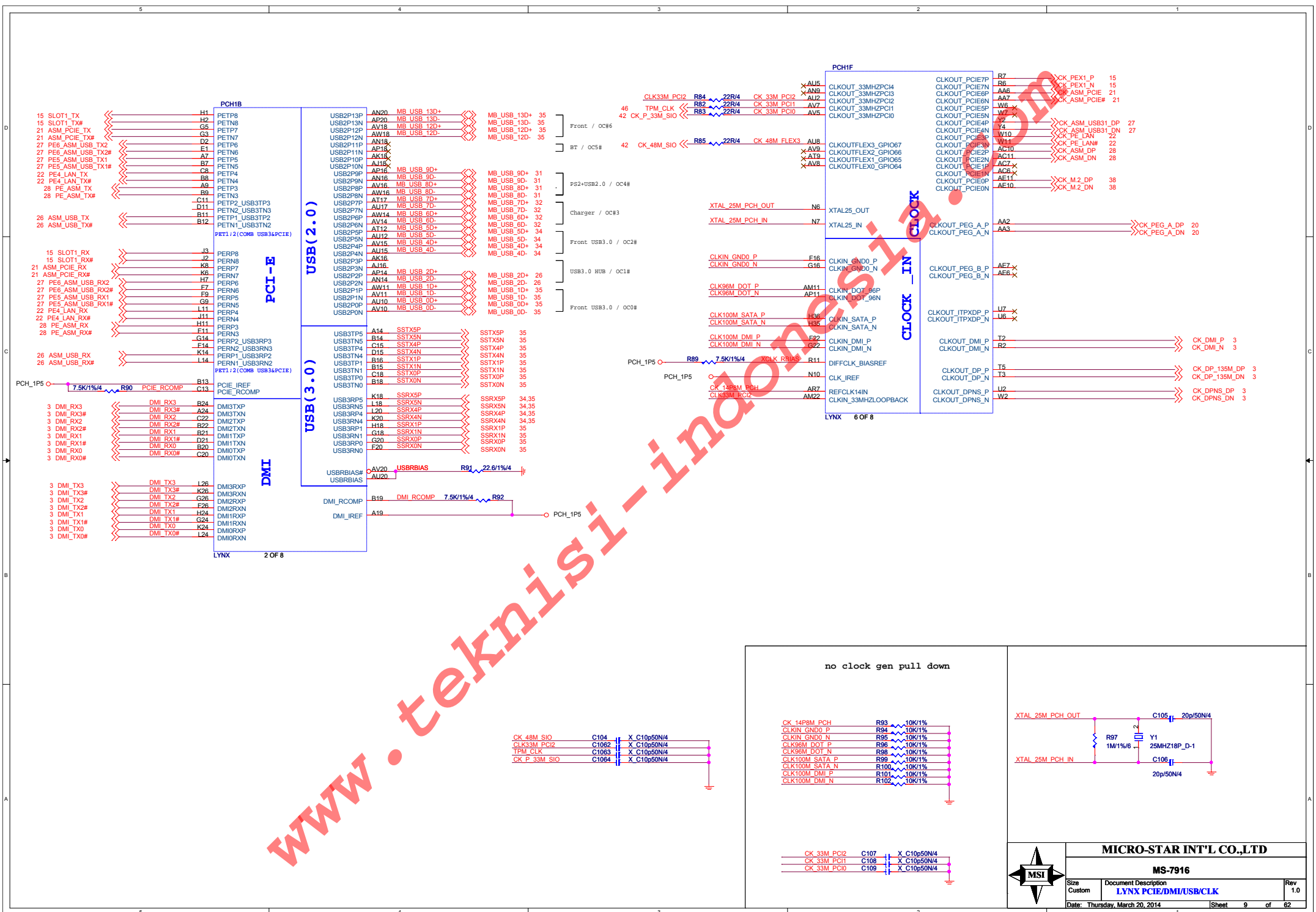
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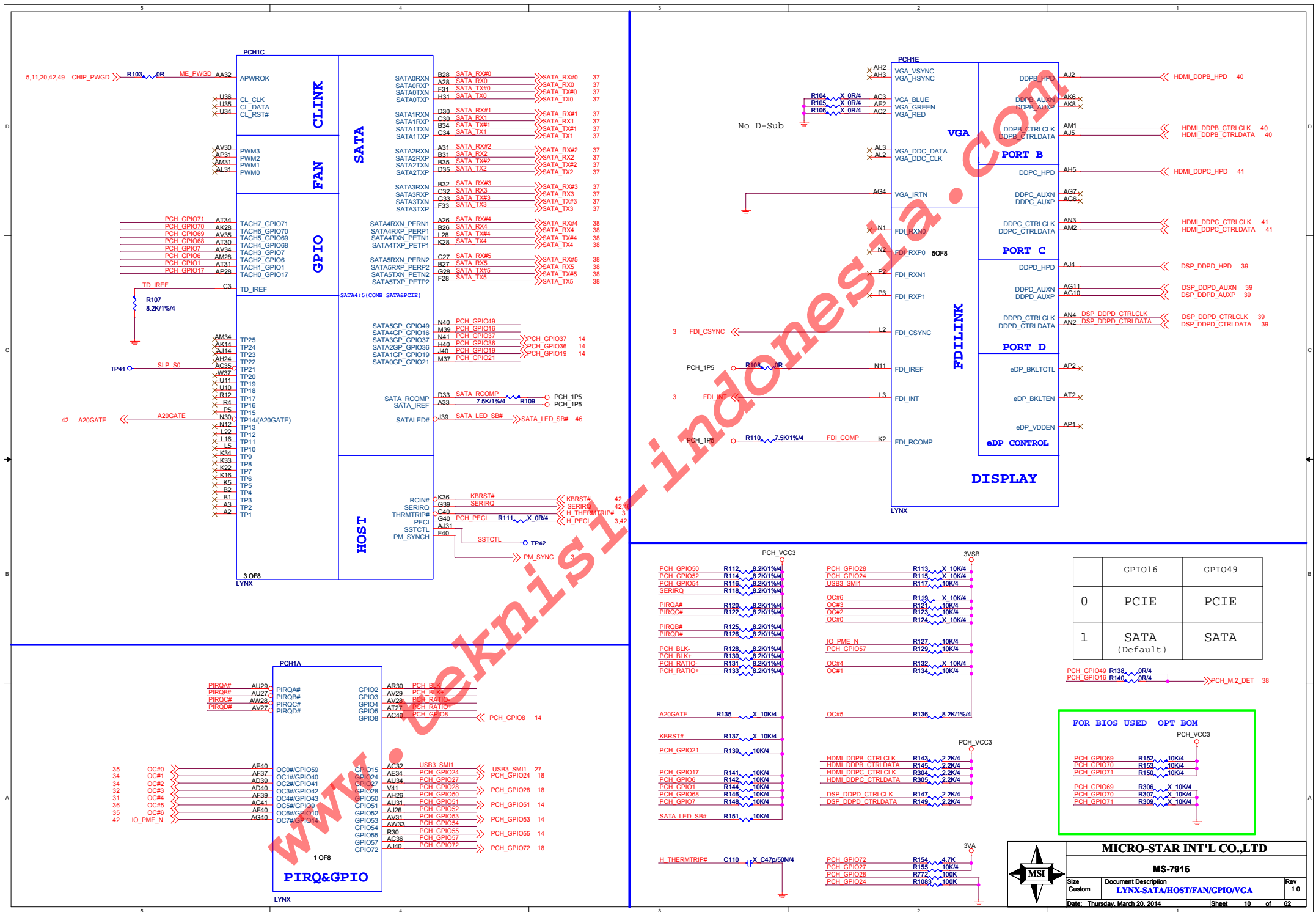
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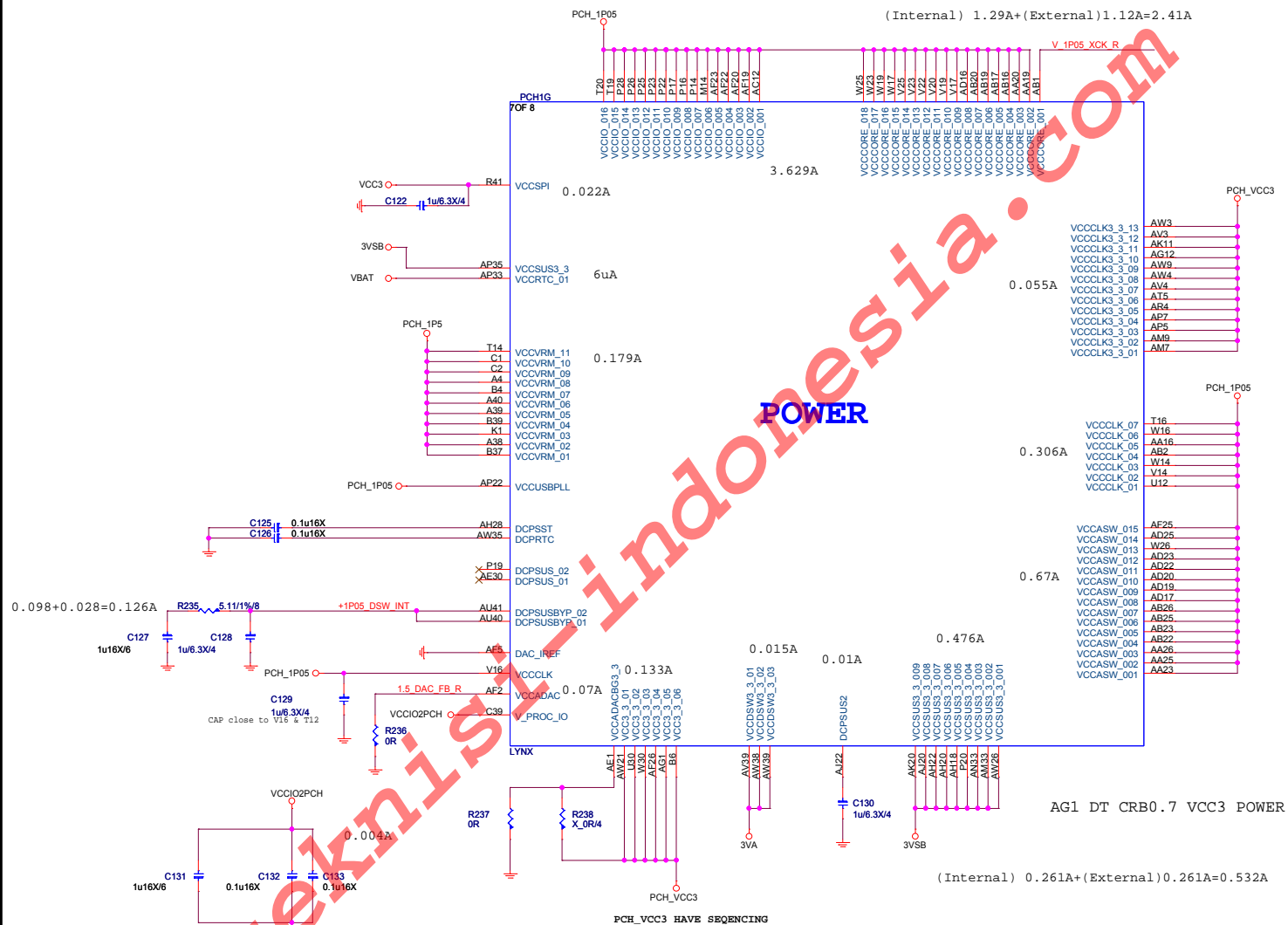
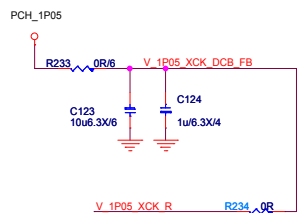
Document Description

Size Custom	Document Description DDR3 Chane-A DIMM1/2	Rev 1.0
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The schematic diagram illustrates the power supply circuit for the PCH_1P05 module. It shows the connection from the PCH_1P05 pin headers to various internal components:

- PCH_1P05 Pin Headers:** C81, C82, C83, C84, C85, C86, C87, C88, C89, C90.
- VBAT:** Connected to C82.
- 3VSB:** Connected to C89.
- PCH_VCC3:** Connected to C88.
- PCH_1P5:** Connected to C87.
- 3VA:** Connected to C88.

The internal components include capacitors (C81-C90) and resistors (R81-R90) connected to ground or other pins. The values are as follows:

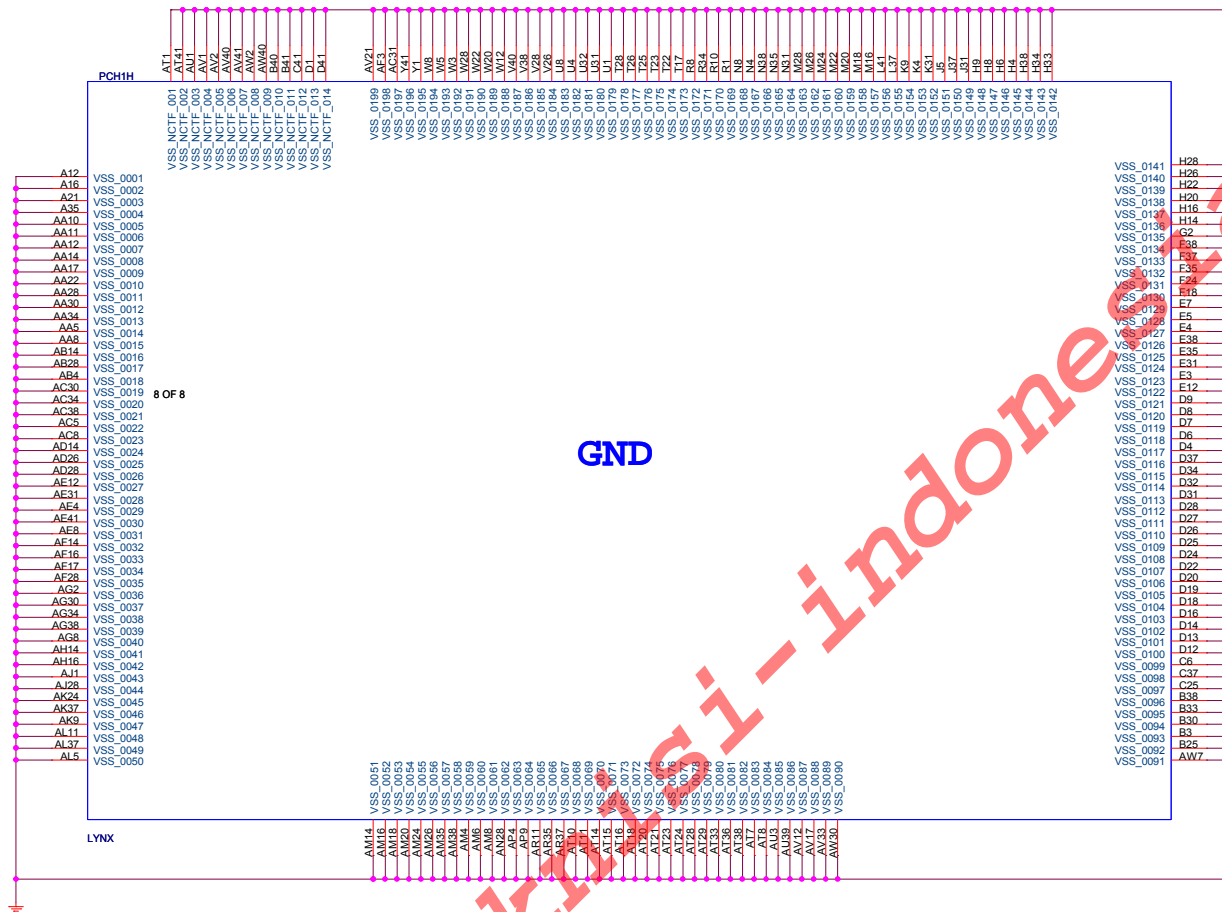
Component	Value
C81	100k 3V6
C82	100k 3V6
C83	100k 3V6
C84	100k 3V6
C85	100k 3V6
C86	100k 3V6
C87	0.1uF 10X
C88	0.1uF 10X
C89	0.1uF 10X
C90	0.1uF 10X



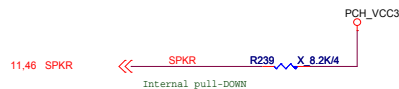
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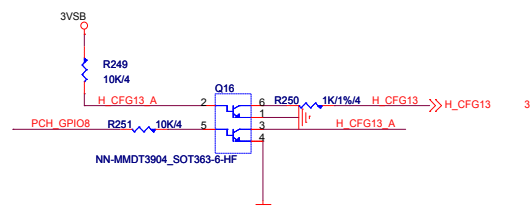
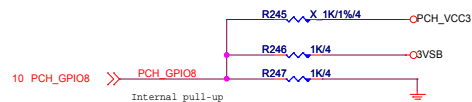
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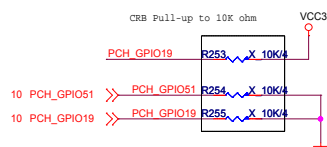


GPIO8



GPIO19 & GPIO51

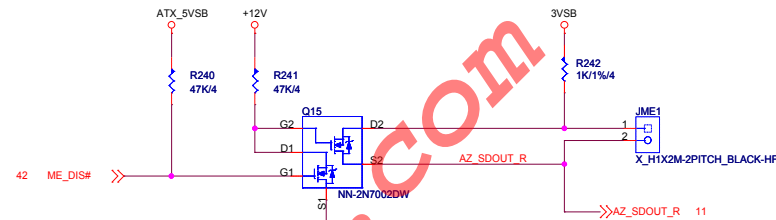
BOOT DEVICE	GPIO51	GPIO19
LPC	0	0
SPI	1	1



Default (SPI):
Left both SATA1GP/GPIO19 and GPIO51 floating.
No pull up required.

Boot from PCI:
Connect SATA1GP/GPIO19 to ground with 1k Ohm pull-down resistor.
Leave GPIO51 Floating.

Boot from LPC:
Connect both SATA1GP/GPIO19 and GPIO51 to ground with 1k Ohm pull-down resistor.

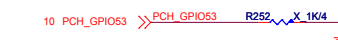


GPIO55

TOP BLOOCK SWAP MODE

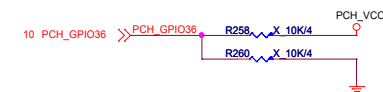
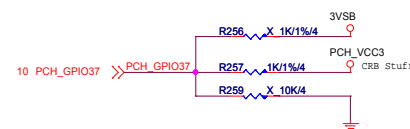
GPIO55
Default Mode:
Internal pull-up.

Top Block Swap Mode:
Connect to ground with 4.7k Ohm weak pulldown resistor.



GPIO53
Connect to ground with 1k Ohm pull-down resistor.

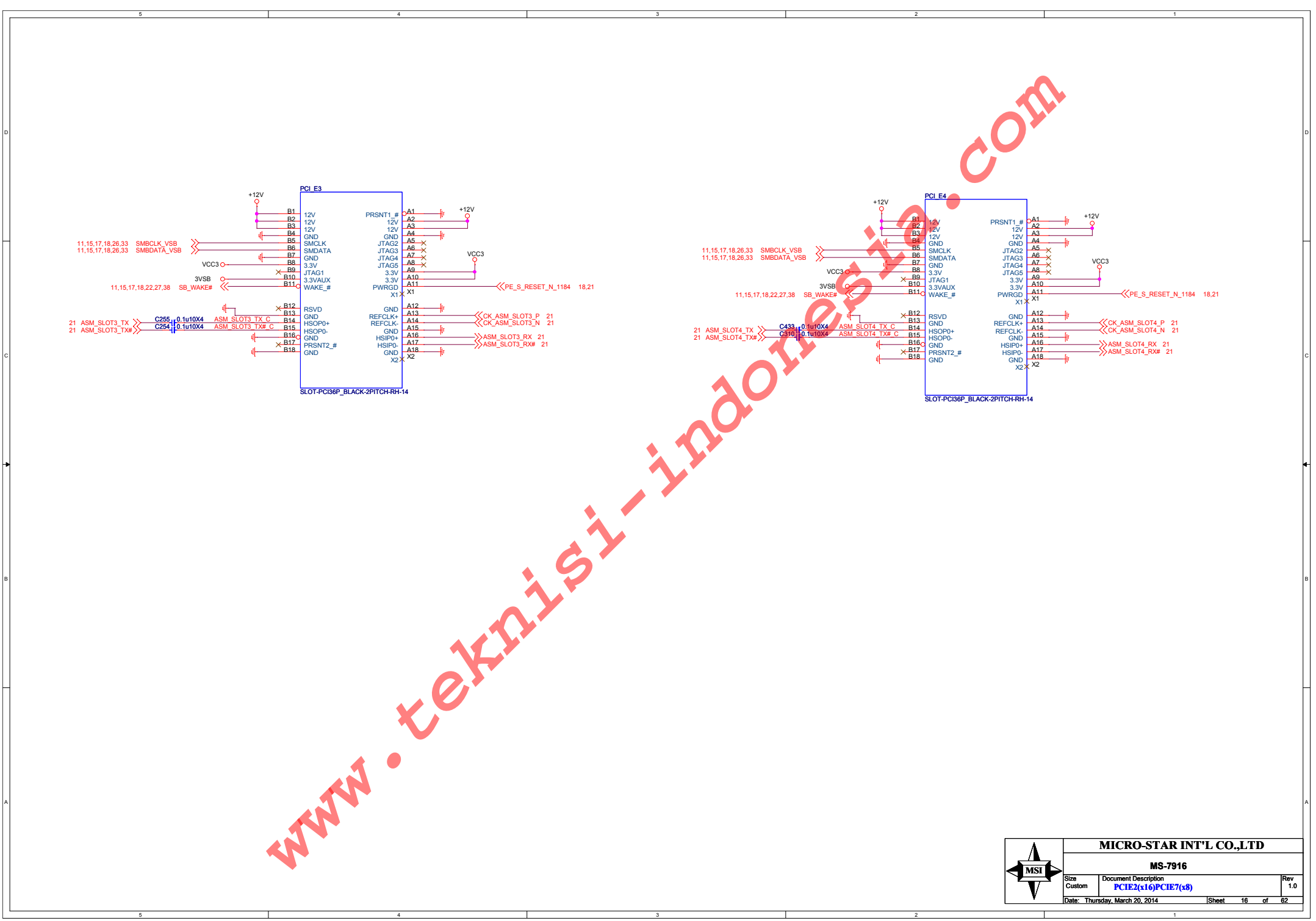
GPIO36 & GPIO37



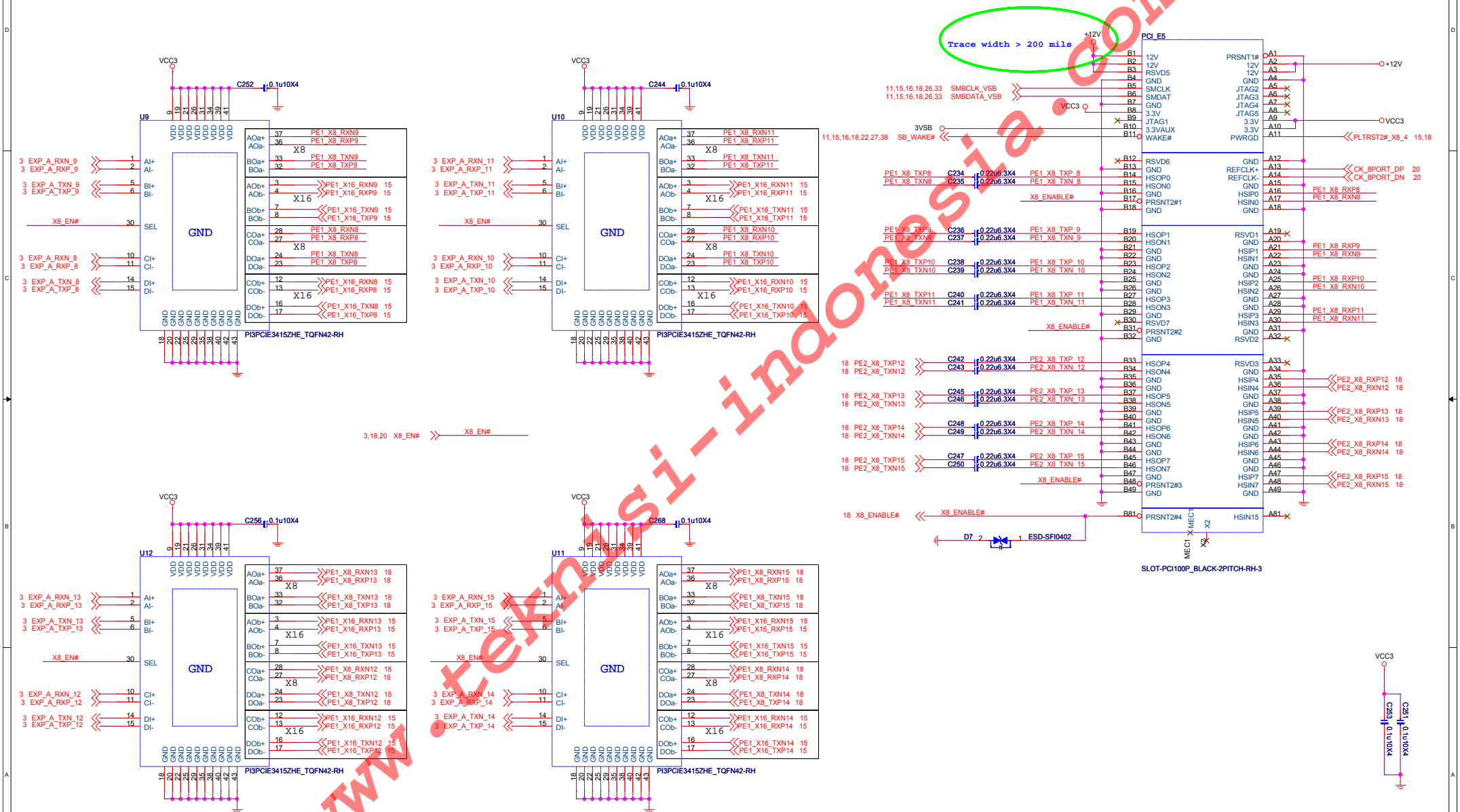
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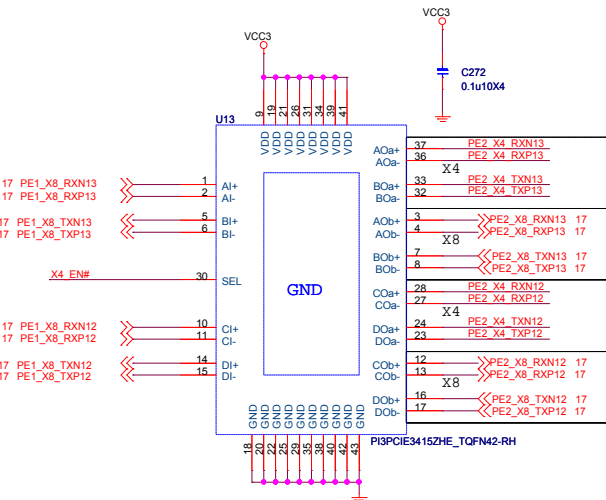
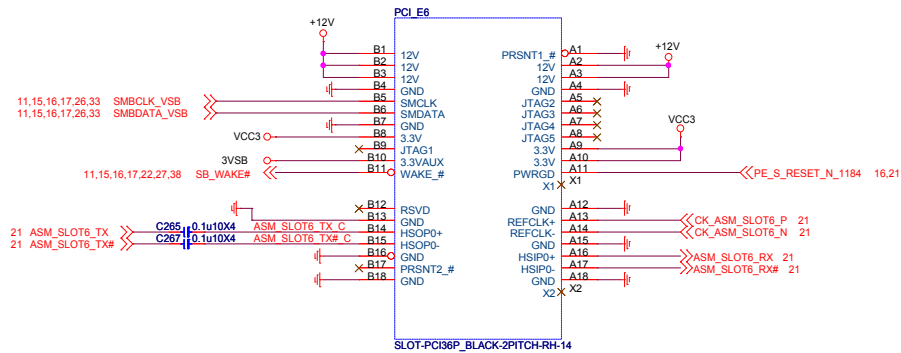
PCI_Express X8 Slot
(Share with PCI_E x16 Slots)



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Size Custom	Document Description PCIE3(X8)PCIE7(x8) SLOT	Rev 1.0
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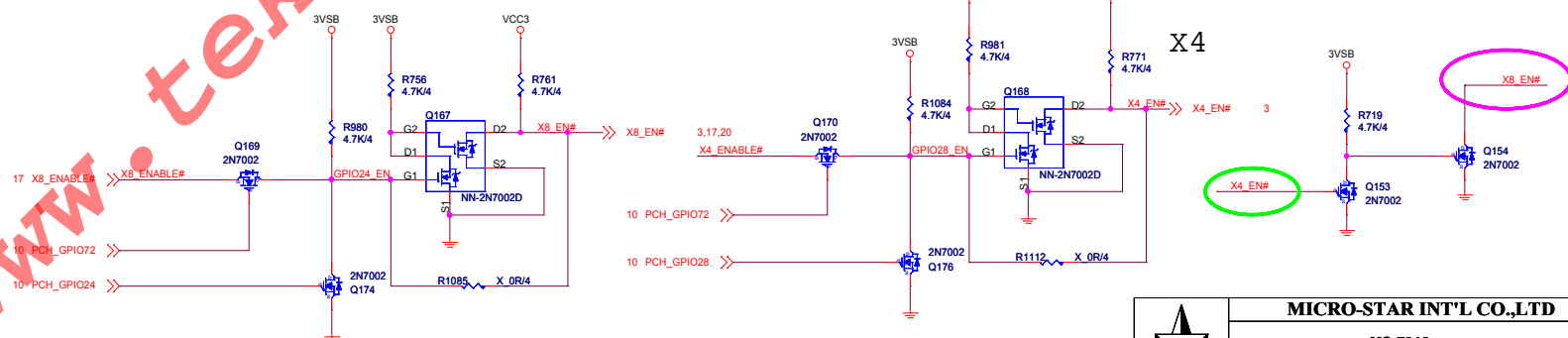
GPIO72

0: BIOS MODE
1: HW MODE

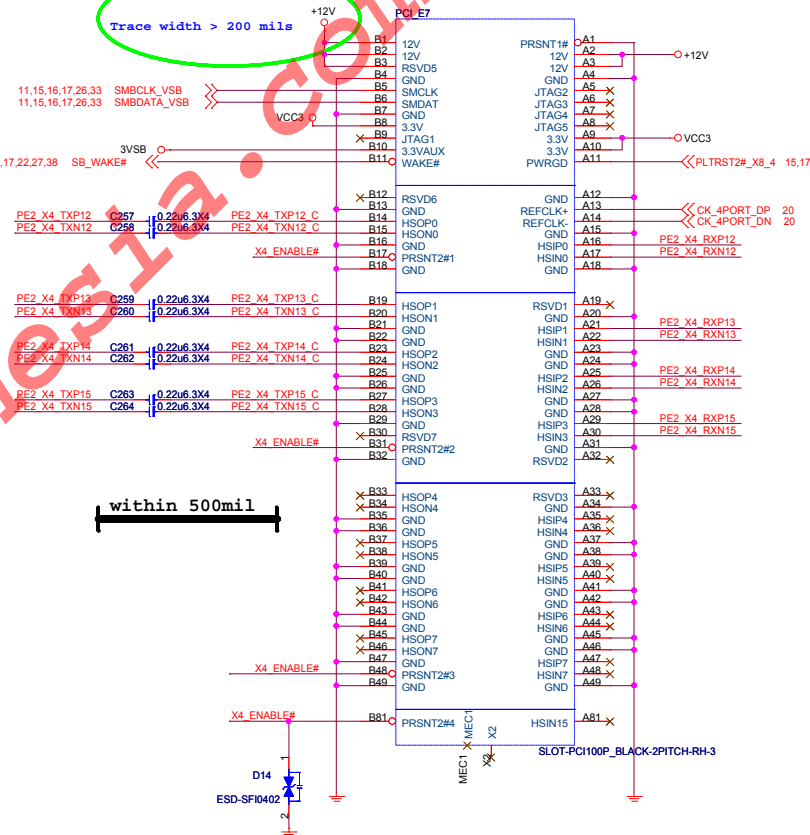
If USE HW MODE (Default)
PCH_GPIO24 & PCH_GPIO28 programming to GPI
PCH_GPIO72 programming to GPO

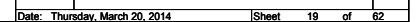
If USE BIOS MODE
PCH_GPIO24 & PCH_GPIO28 & PCH_GPIO70
programming to GPO

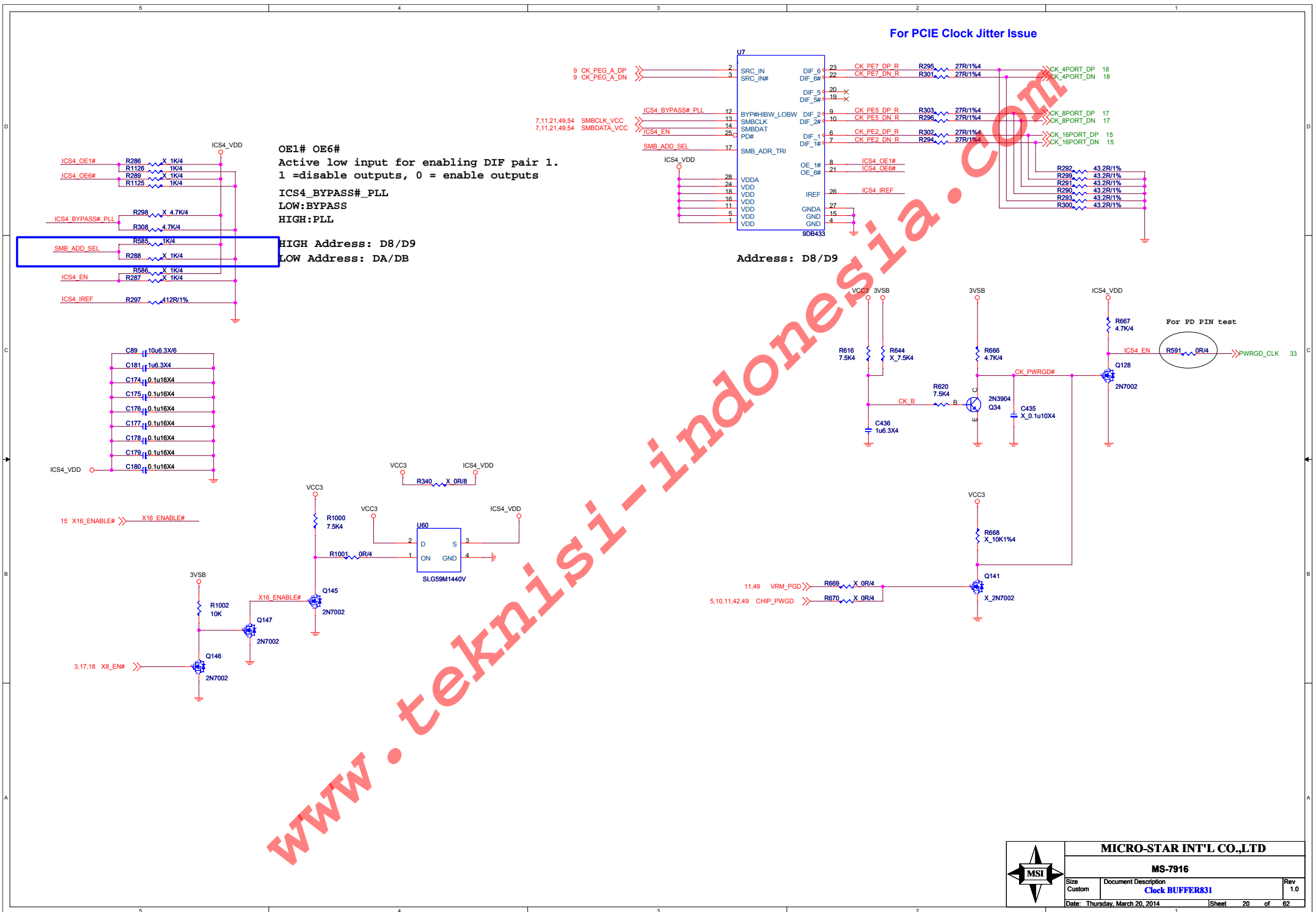
PCH Status	GPIO24	GPIO28	GPIO72
AUTO	GPI	GPI	1
16,0,0	0	0	0
8,8,0	1	0	0
8,4,4	1	1	0



PCI Express X4 Slot(by CPU)





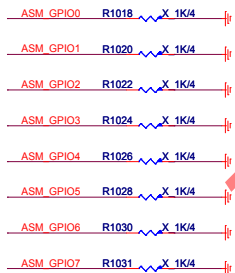


GPI00	0:PLL mode; 1: bypass mode
GPI01	clock buffer termination 0: disable ; 1: enable
GPI02	Reserved for test mode
GPI03	Reserved for ASM1184e
GPI04	SMBus enable
GPI05	SMBus address[0]
GPI06	SMBus address[1]
GPI07	SMBus address[2]
MSCL	I2C enable

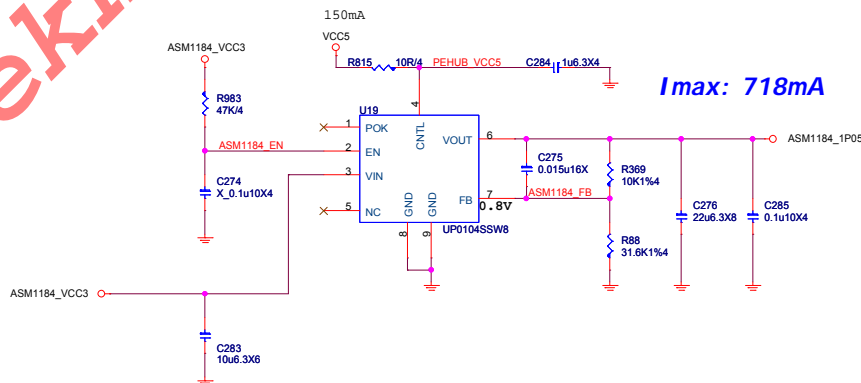
GPI04	MSCL	Function
0	0	(MSCL,MSDA) is no function
0	1	(MSCL,MSDA) is I2C,chip is master
1	0	(MSCL,MSDA) is SMBus, chip is salve
1	1	(MSCL,MSDA) is SMBus, chip is salve

H/W Strapping

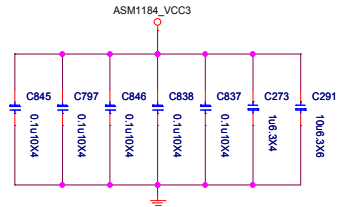
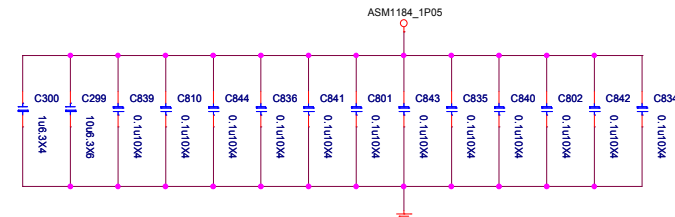
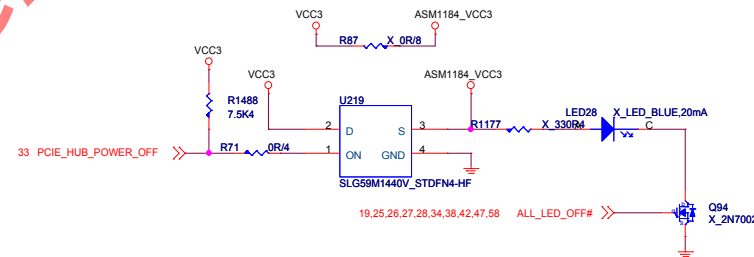
Internal pull high 50Kohm



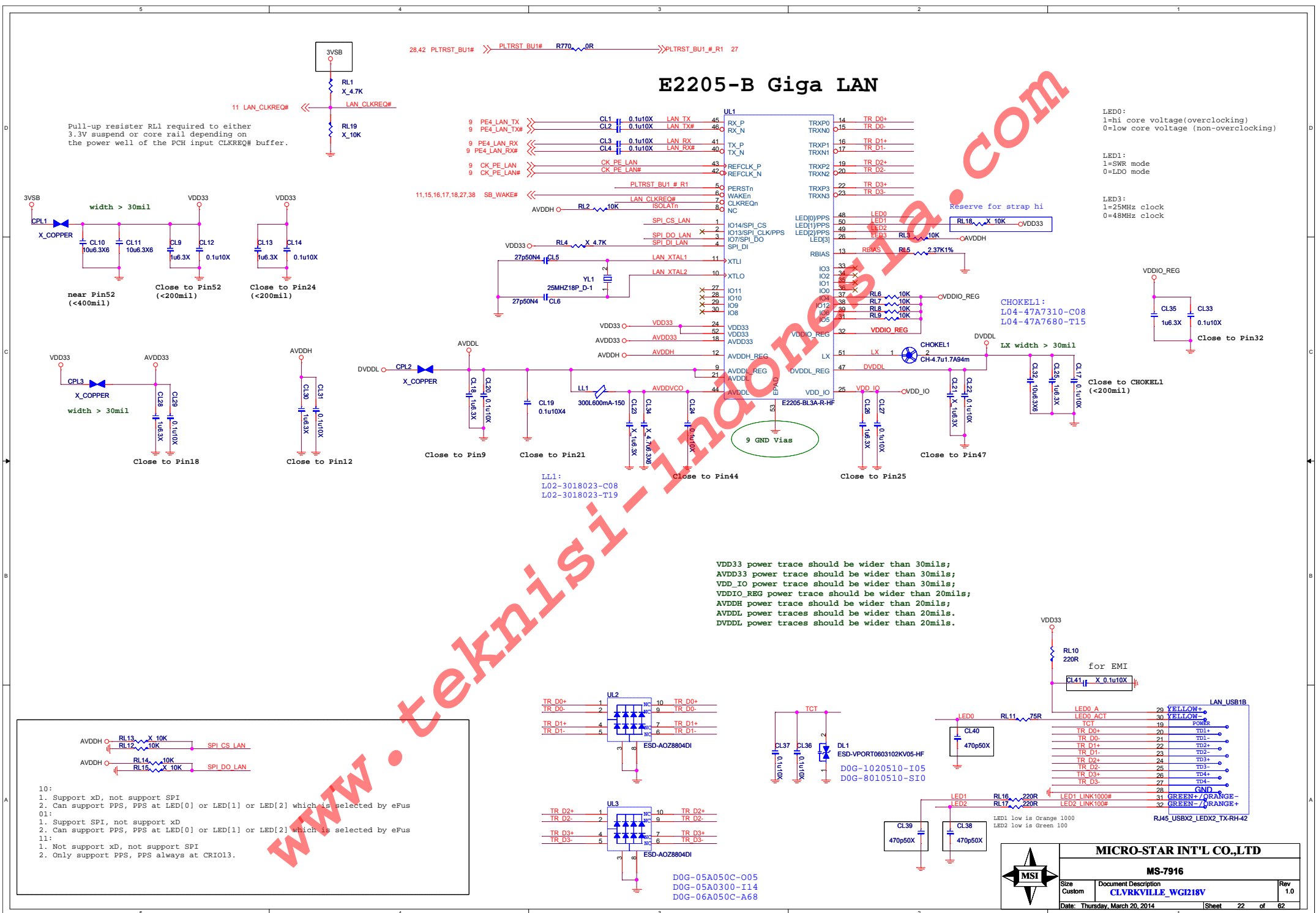
ASM1184 PCIe HUB core Power



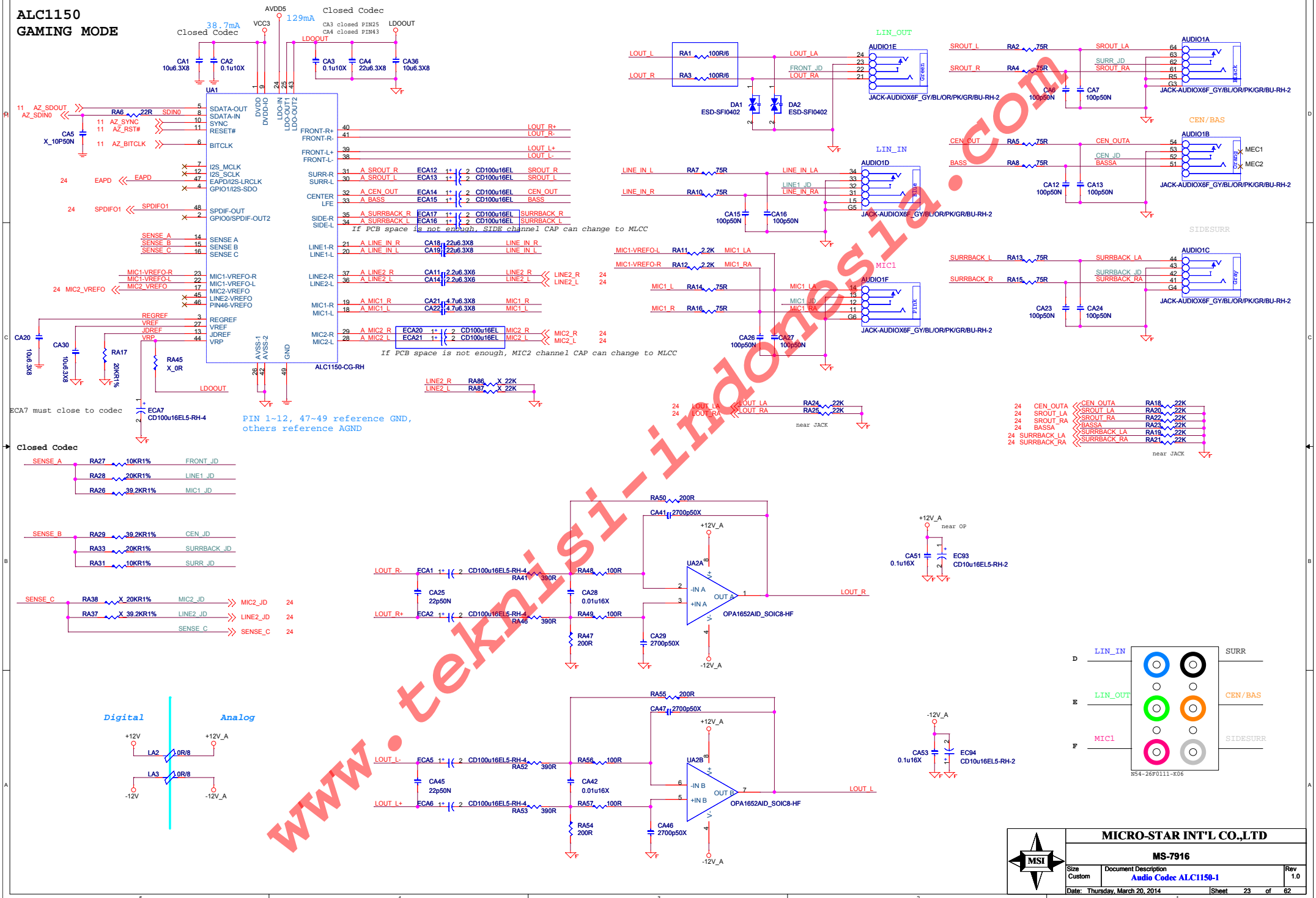
PCIe HUB power switch



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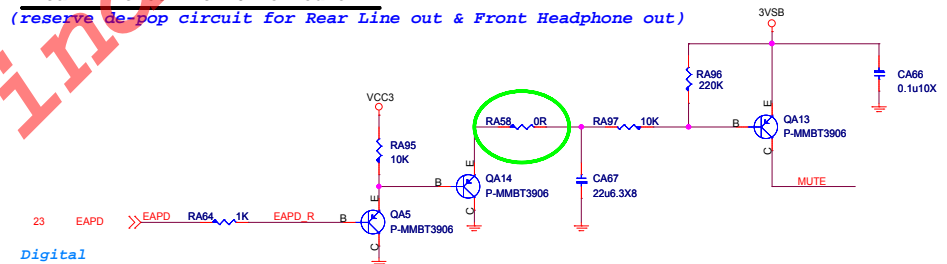
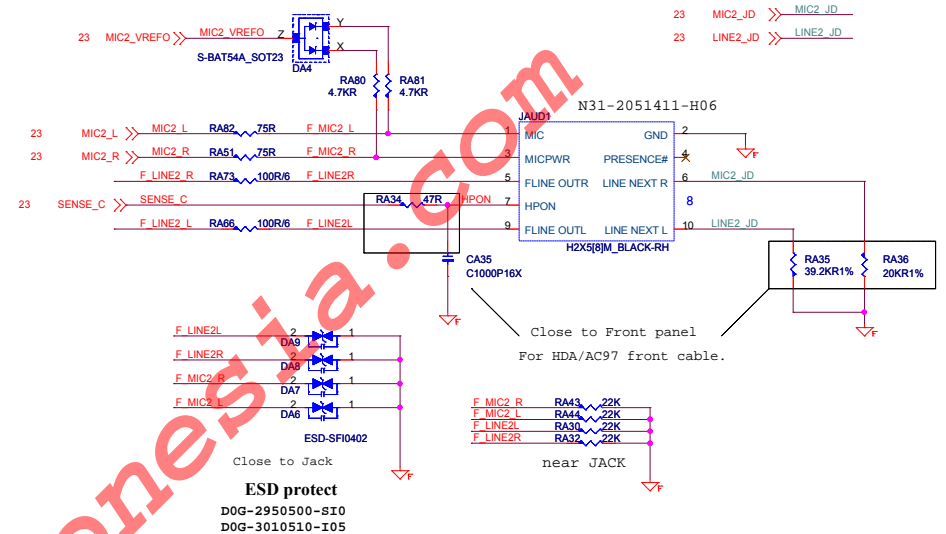
ALC1150
GAMING MODE



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Size Custom	Document Description Audio Codec ALC1150-I	Rev 1.0
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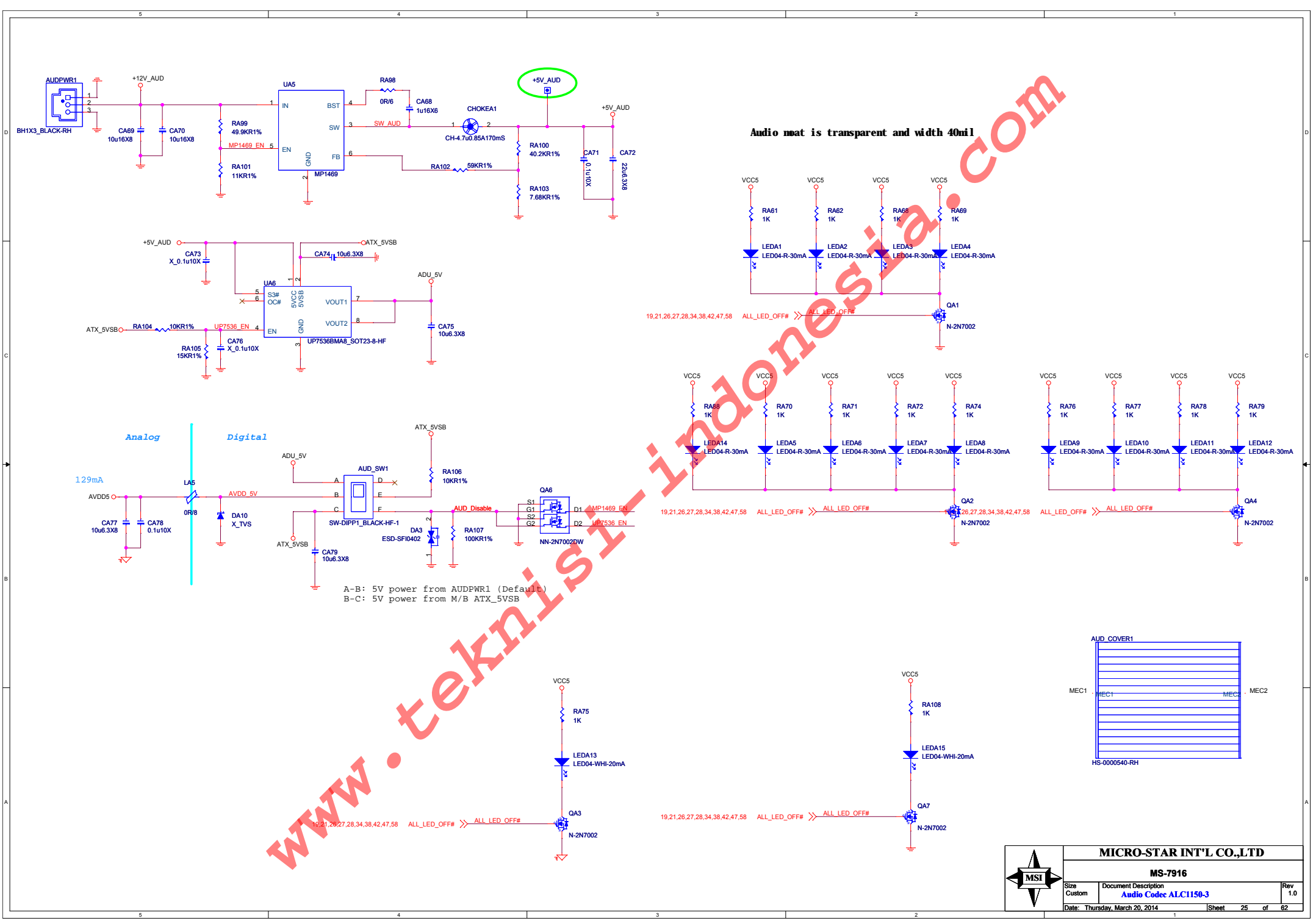


Component	Value
QA9	23
QA10	23
QA11	23
RA83	X 1K
RA85	X 1K
RA89	X 1K
RA90	X 1K
RA91	X 1K
RA92	X 1K



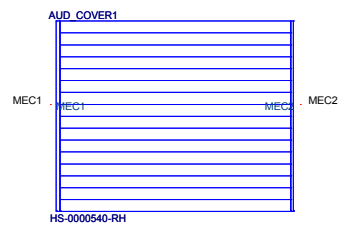
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Size Custom	Document Description Audio Codec ALC1150-2	Rev 1.0
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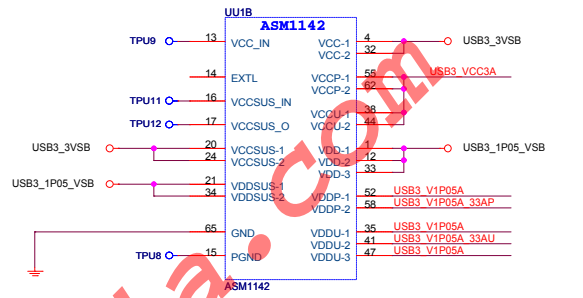
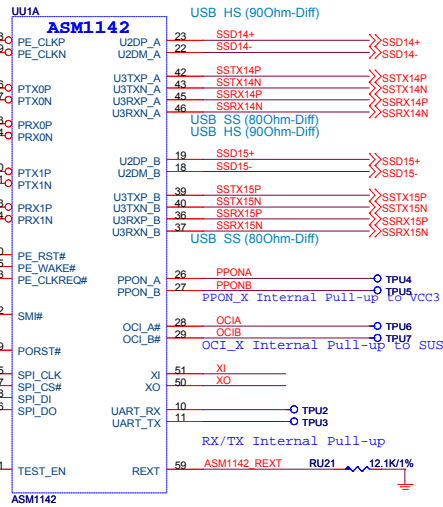
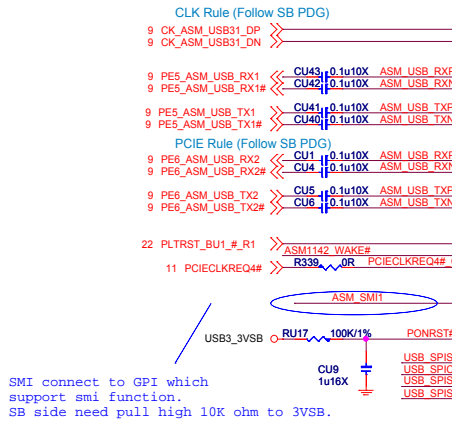
Audio meat is transparent and width 40mil

A-B: 5V power from AUDPWR1 (Default)
B-C: 5V power from M/B ATX_5VSB



Minimum gap should be greater of
>15mil with other signal.

3.3V: 95mA
3.3VSUS: 6.6mA
1.05V: 300mA
1.05VSUS: 5.8mA



ASM1061 SATA6G

22.42 PLTRST_BU1# >> PLTRST_BU1# R774 0R >> PLTRST_BU1#_R2 21.46

9 PE_ASM_TX >> CS3 0.1u16X4 ASM_TX#_C 31 PRXP
9 PE_ASM_TX# >> CS1 0.1u16X4 ASM_TX#_C 32 PRXN
9 PE_ASM_RX >> CS4 0.1u16X4 ASM_RX#_C 34 PTXP
9 PE_ASM_RX# >> CS2 0.1u16X4 ASM_RX#_C 35 PTXN

9 CK_ASM_DP >> 26 PECLKP
9 CK_ASM_DN >> 27 PECLKN

21.46 PLTRST_BU1#_R2 >> R786 0R 45 PERST#

RS1 12.1K1%4 PREXT 37 PREXT

TPSO SATA_SPL_CLK 38 SPI_CLK

TPS2 SATA_SPL_DO 40 SPI_DO

TPS3 SATA_SPL_DI 41 SPI_DI

46 ASM_HD_LED# >> ASM_HD_LED# 46 LED

TESTMODE ASM1061_VCC3 >> RS3 X 4.7K/4 47 TESTMODE
0: Disable
1: Enable

CPS1 X COPPER 3 VCC33IN

TPS7 2 EXT_L

CPS2 X COPPER 1 VSSPWM

Add- 2011.8.15

Remove ASM1061 internal power solution

ASM1061

SRXP_A 24 >> ASATA_RXP0 37
SRXN_A 23 >> ASATA_RXN0 37
STXP_A 20 >> ASATA_TXP0 37
STXN_A 21 >> ASATA_TXN0 37

SRXP_B 13 >> ASATA_RXP1 37
SRXN_B 14 >> ASATA_RXN1 37
STXP_B 17 >> ASATA_TXP1 37
STXN_B 16 >> ASATA_TXN1 37

29 XI SATA_6G
28 XO SATA_6G

SREXT 18 >> RS2 12.1K1%4

VC33 9 >> ASM1061_VCC3

VC33P 36 >> VCC33P

VC33S 19 >> VCC33S

VCC12 7 >> VCC12P25

VCC12 11 >> VCC12S

VCC12 43 >> VCC12S

VCC12 48 >> VCC12S

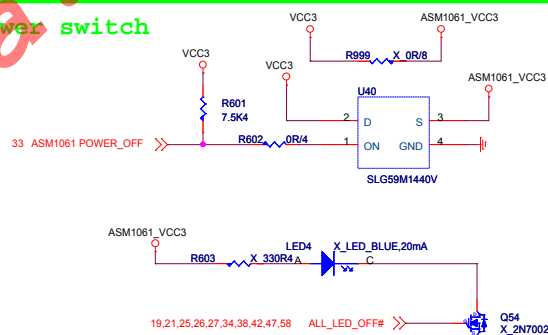
VCC12P 30 >> VCC125P

VCC12S 12 >> VCC125S

VCC12S 25 >> VCC125S

ASM1061

ASM SATA power switch



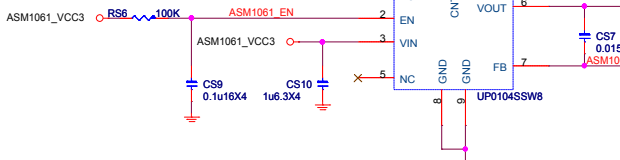
1.2V delay from 3.3V 90% > 0ms

VCC5 >> RS5 10R ASM1061_VCC CS6 1u6.3X4

330 mA

ASM1061 POWER Consumption

	3.3V	1.2V	Power (mW)
Idle (mA)	98.45	212.3	579.645
Busy (mA)	91.1	330.7	697.47



ASM1061_VCC3 >> LS1 0R/8 >> VCC33P

CS11 0.1u10X4

CS12 0.1u10X4

CS13 0.1u10X4

Place near pin 9,44

Place near pin 35

VCC12P25 >> LS2 0R/8 >> VCC125P

CS14 0.1u10X4

CS15 0.1u10X4

CS16 0.1u10X4

CS17 0.1u10X4

CS18 0.1u10X4

Place near pin 7,11,43,48

Place near pin 30

ASM1061_VCC3 >> LS3 0R/8 >> VCC33S

CS19 0.1u10X4

Place near pin 19

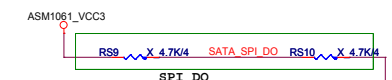
VCC12P25 >> LS4 0R/8 >> VCC125S

CS20 0.1u10X4

CS21 0.1u10X4

Place near pin 12,25

3.0



0: Spinup by H/W
1: Spinup by S/W

Add- 2011.3.18

SATA_SPL_DO don't need pull up (integrated pull-up)
or pull down for Asmedia recommendation.
Asmedia suggest that we use spinup by s/w mode for MB or PCI-E Card.




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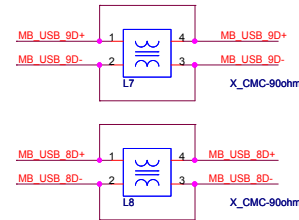
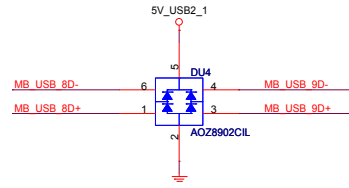
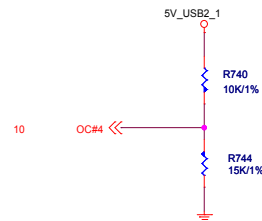
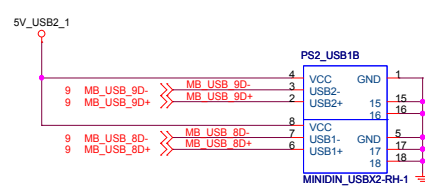
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	MS-7916				
	Size	Document Description			Rev
	Custom	Clock GEN IDR5901			1.0
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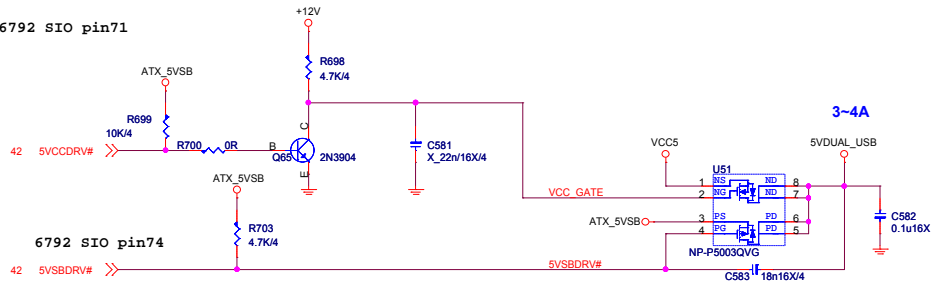
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Size	Document Number		
Custom	<Doc>		
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REAR USB PORT 8,9 (With PS2)

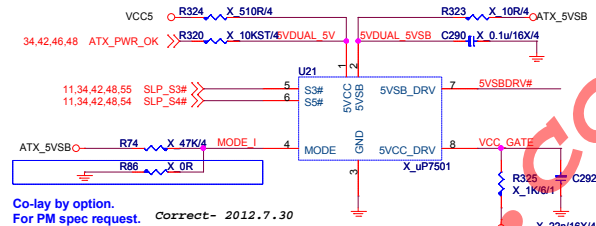


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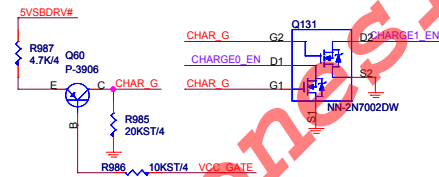
6792 SIO pin71



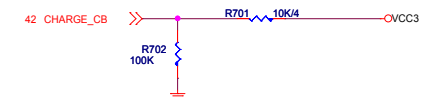
5VDUAL_USB - uP7501



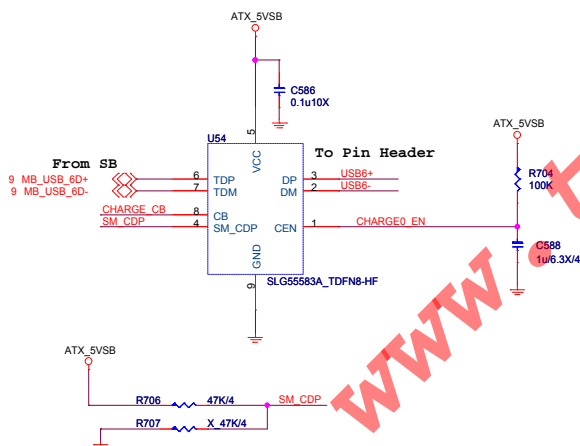
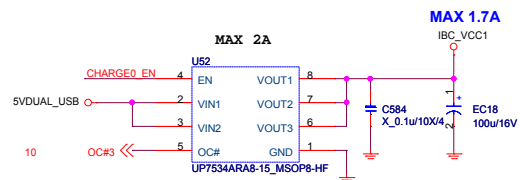
Co-lay by option.
For PM spec request. Correct- 2012.7.30



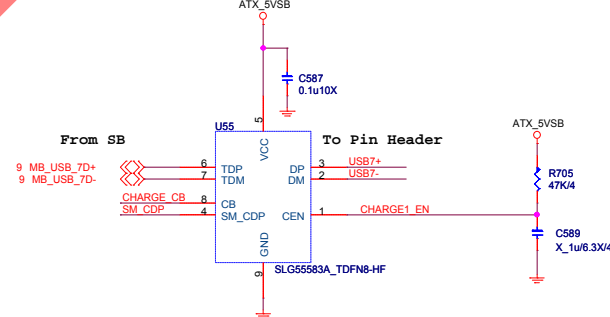
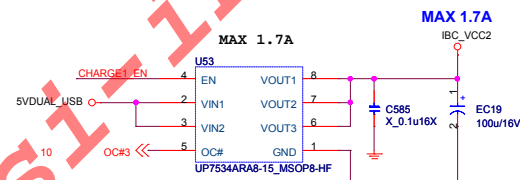
Pin power : I_3VSB
Register power : I_3VSB
Register reset : I_3VSB



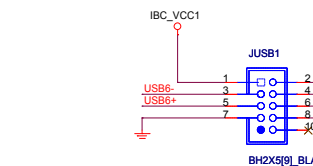
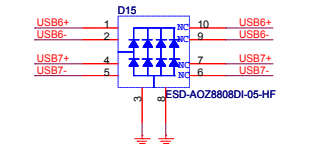
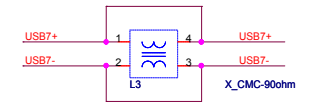
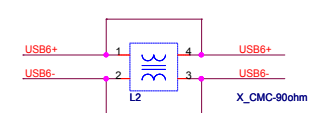
USB POWER PORT 0 For USB Charging



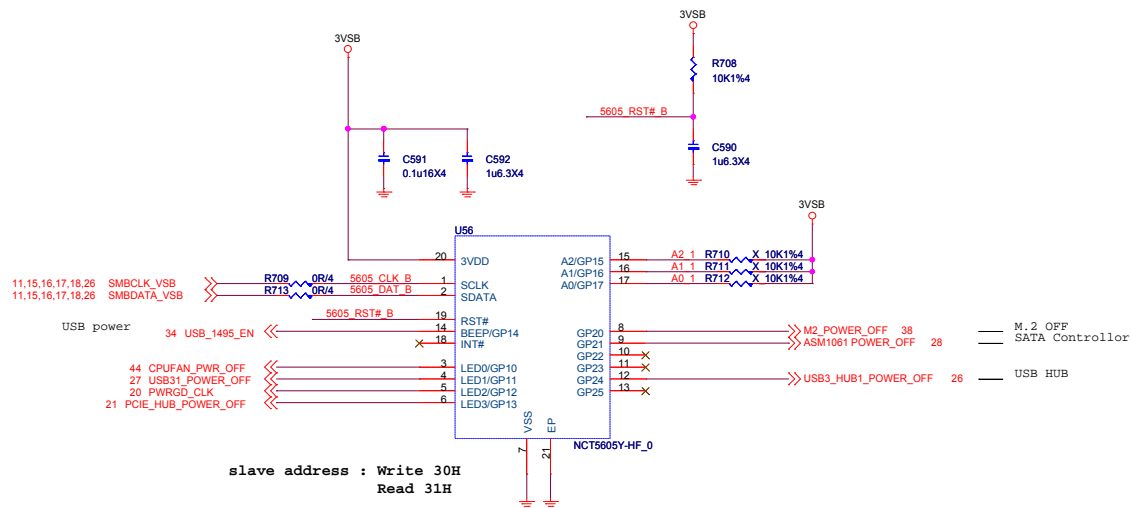
USB POWER PORT 1 For USB Charging



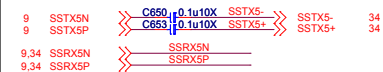
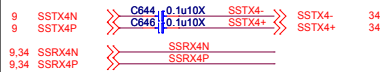
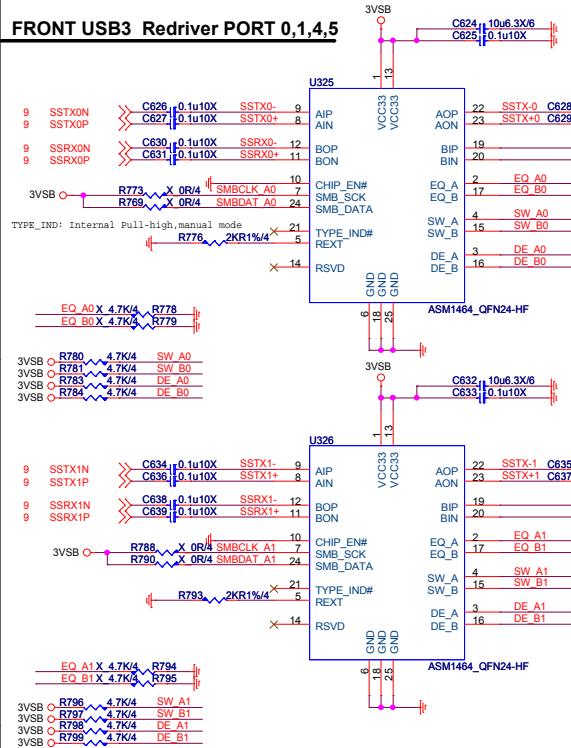
FRONT USB PORT 0,1



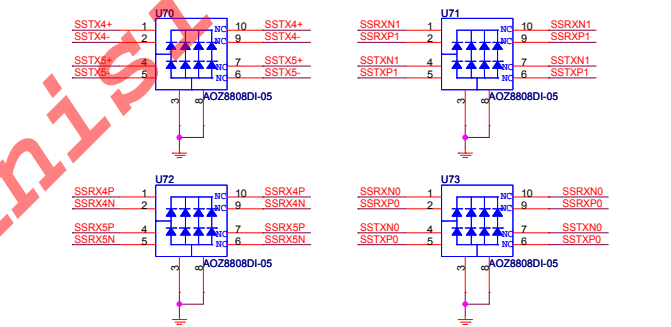
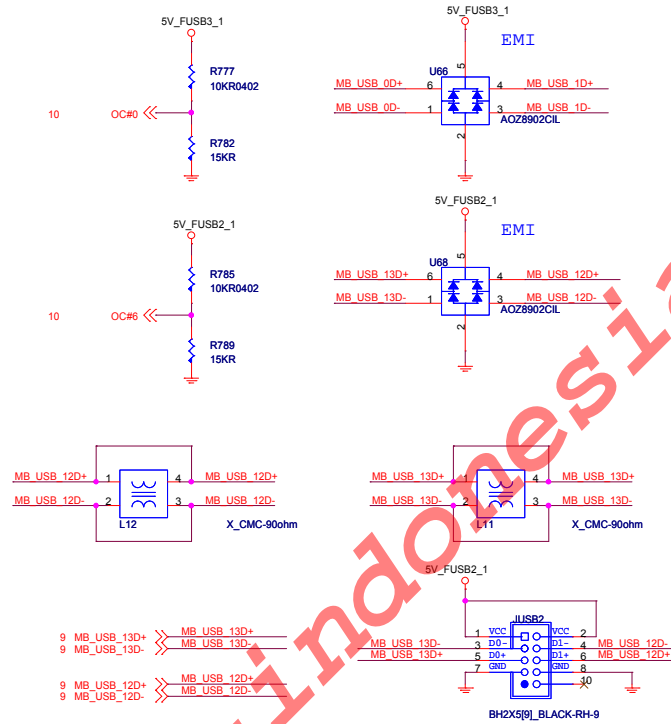
MICRO-STAR INT'L CO.,LTD			
MS-7916			
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Custom	SLG55583A USB CHARGE	1.0	
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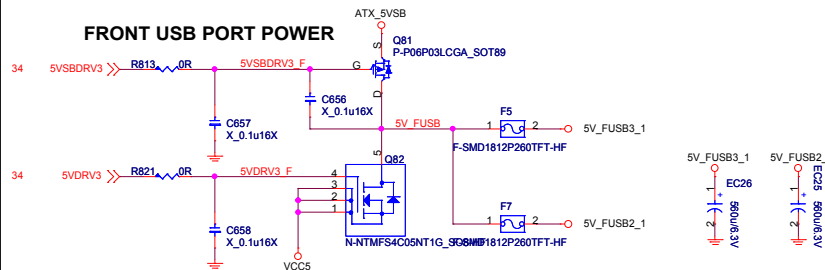
FRONT USB3 Redriver PORT 0,1,4,5



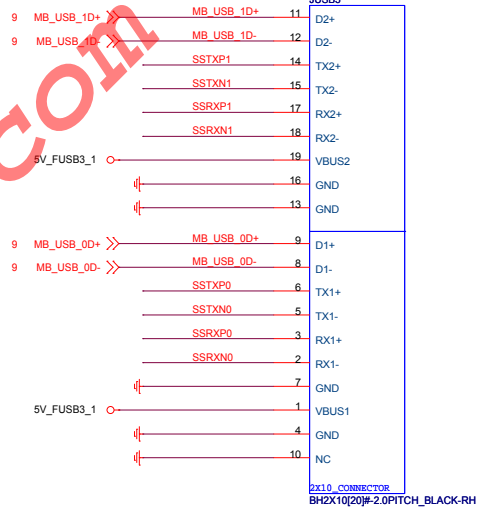
FRONT USB2 PORT 0,1,4,5,12,13



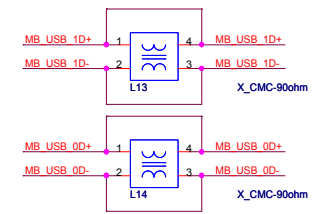
FRONT USB PORT POWER



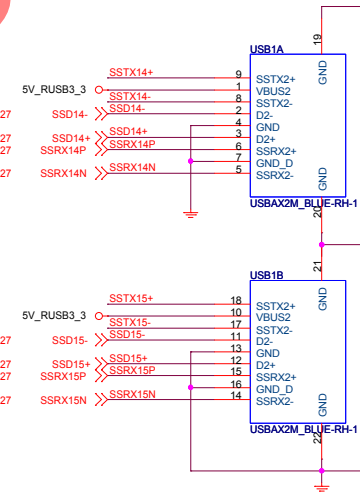
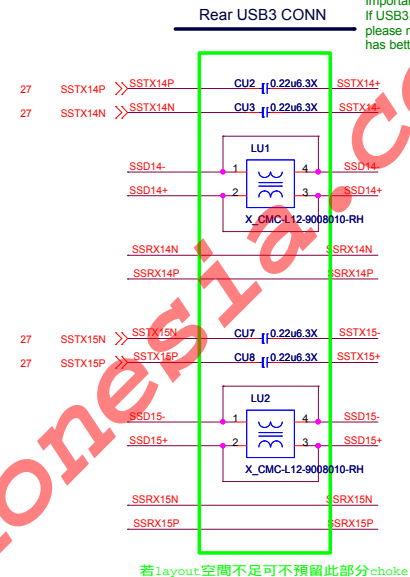
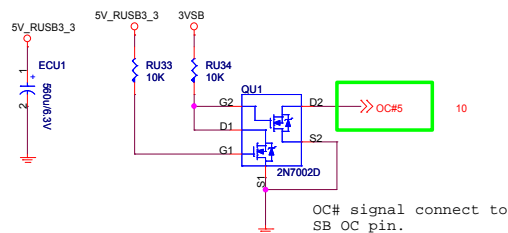
900 mA min 40mil. 900 mA min 40mil.



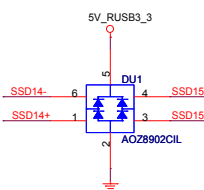
900 mA min 40mil. 900 mA min 40mil.



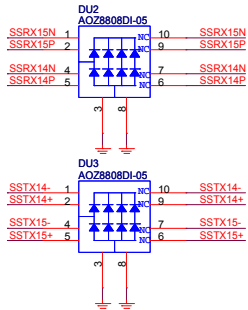
MICRO-STAR INT'L CO.,LTD			
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Size Custom	Document Description	FRONT USB REDRIVER CONNECTOR	
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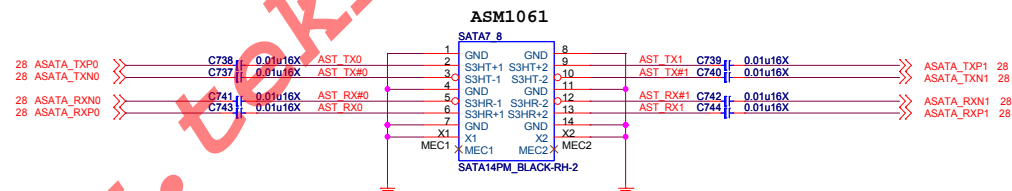
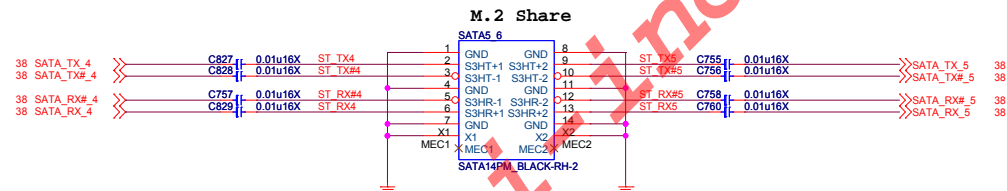
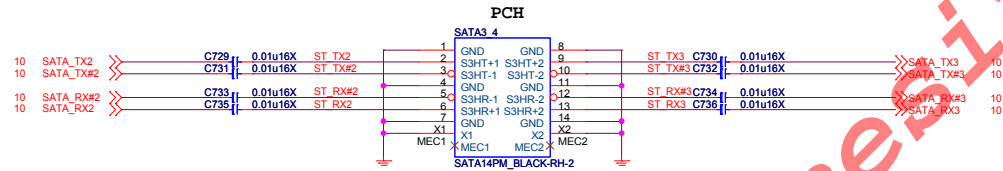
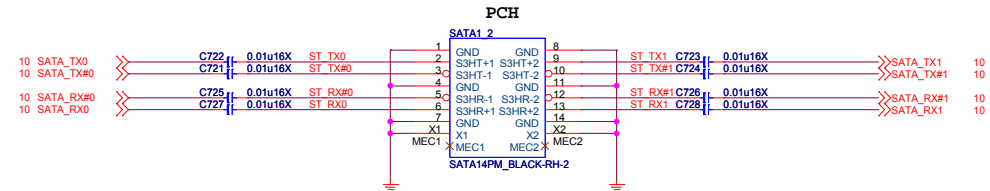
USB2.0
D0G-0200529-A68 Main
D0G-0100619-I05 AVL

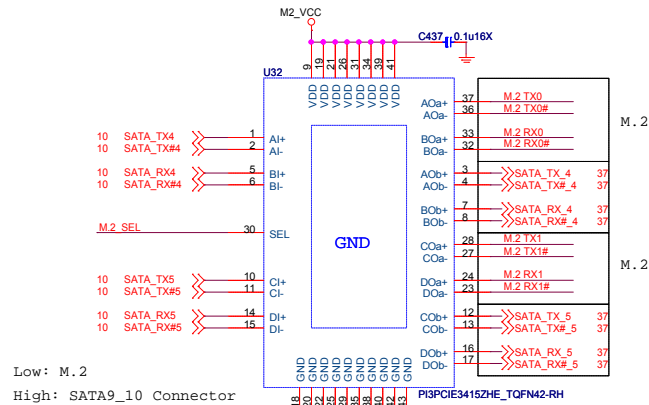


ESD Protection
NEAR CONNECTOR

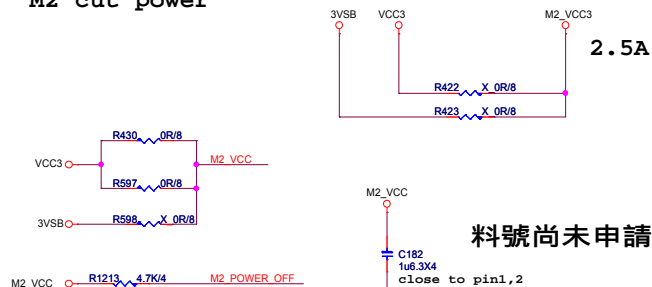


USB3.0
D0G-06A050C-A68 Main
D0G-05A0300-I14 AVL





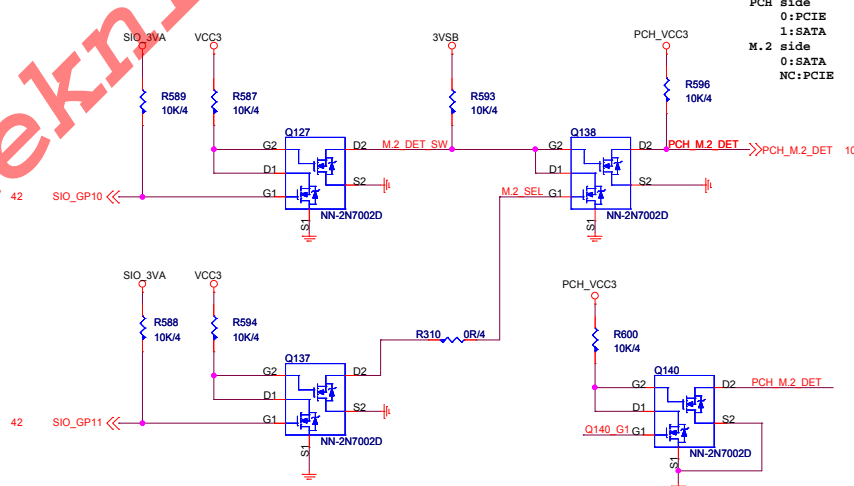
M2 cut power



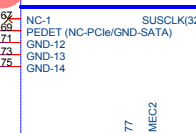
BIOS_MODE

GP10	GP11	PCH_SEL	Mode
0	0	1	M2-SATA
0	1	1	Int-SATA
1	0	0	M2-PCIE
1	1	1	AUTO

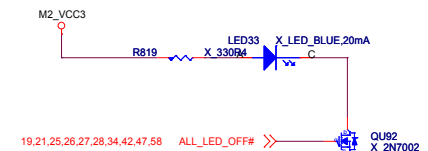
SATA & PCIE SWITCH

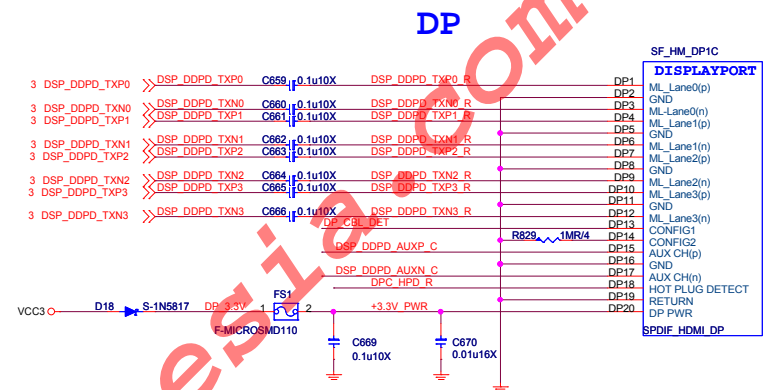
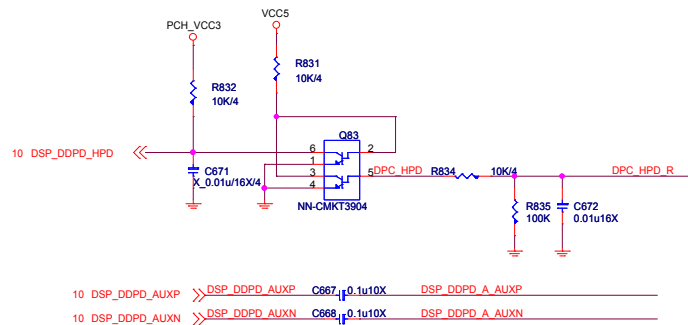


KEY M

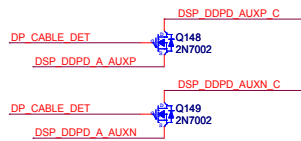


Footprint: H_R256D165_PB

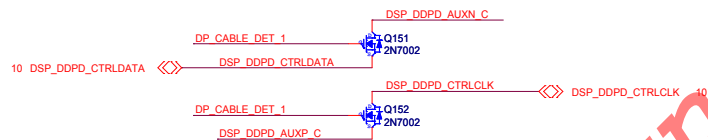




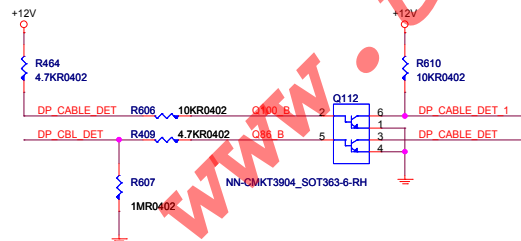
DisplayPort*Interoperability Implementation



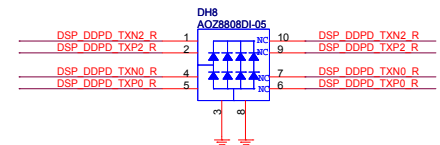
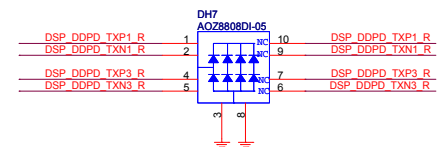
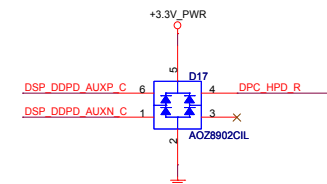
PS:DSP_DDPD_CTRLCLK
PULL HIGH 3.3V 2.2K ohm on chip side



PS:DSP_DDPD_CTRLDATA
PULL HIGH 3.3V 2.2K ohm on chip side



DP_CBL_DET	DP	HDMI
HDMI_C_DNG_DETECT	L	H
DP_DEVICE_DETECT	H	L
HDMI_DEVICE_DETECT	L	H

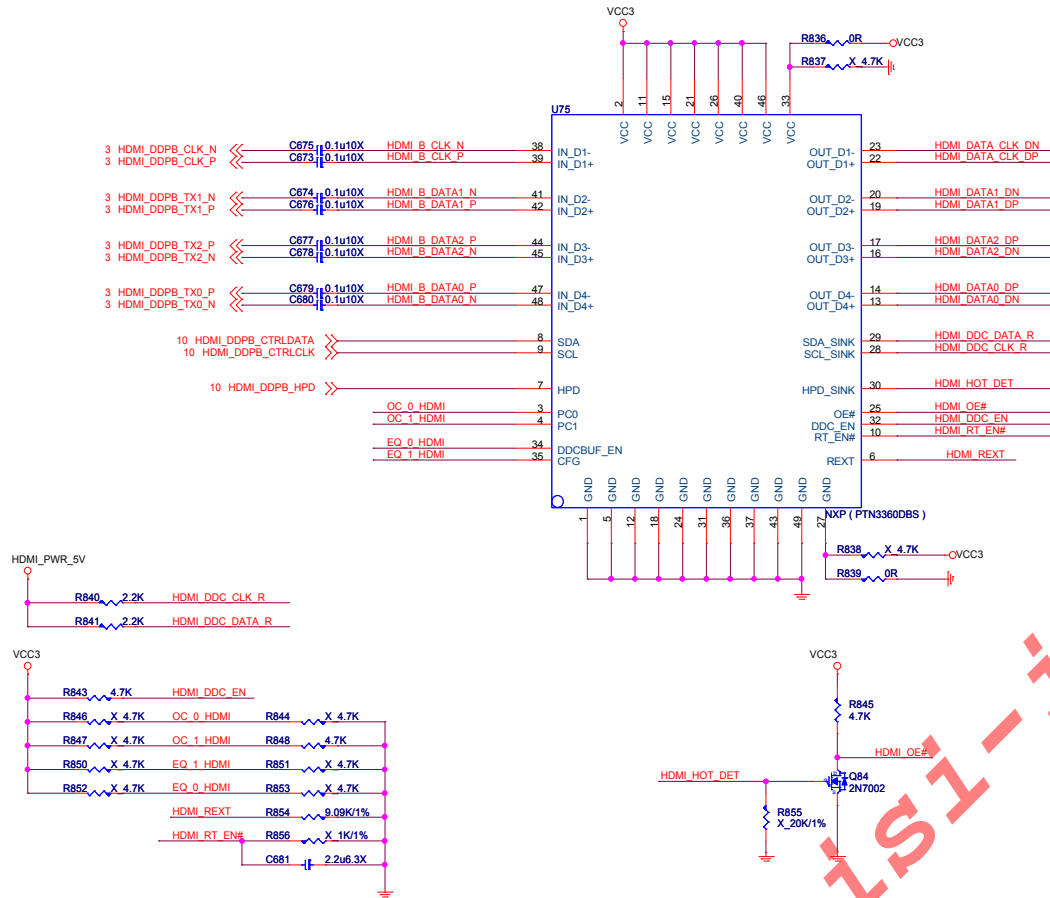


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HDMI level shifter

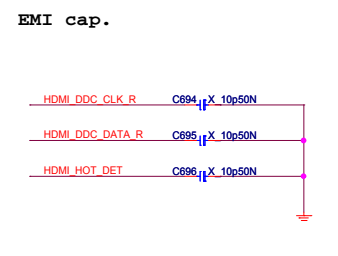
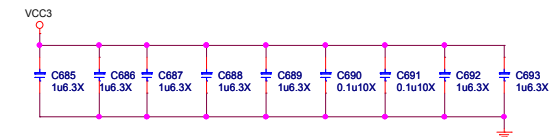
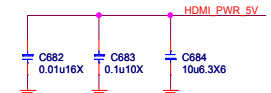
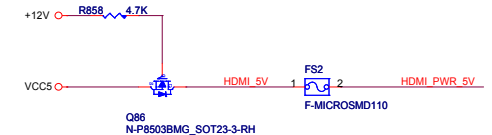
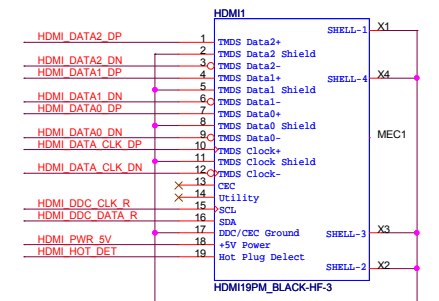


	"0"	"1"	note
DDC_EN	DDC level shifter disable	DDC level shifter enable	internal pull-up at ~500K ohm.
RT_EN#	Input 50 ohm termination resistor enable	the input termination ; resistors are set to high impedances	internal pull-down at ~500K ohm.
OE#	enable	the chip is power down and input termination resistors will be at high impedance.	internal pull-down at ~500K ohm.
HPD_SINK	disable	enable	Internal pull-down at ~200K ohm; 5V tolerant.
DDCBUF_EN	For DDC level shifting configuration, please refer to Table.		internal pull-down at ~500K ohm.
REXT			analog current generation.

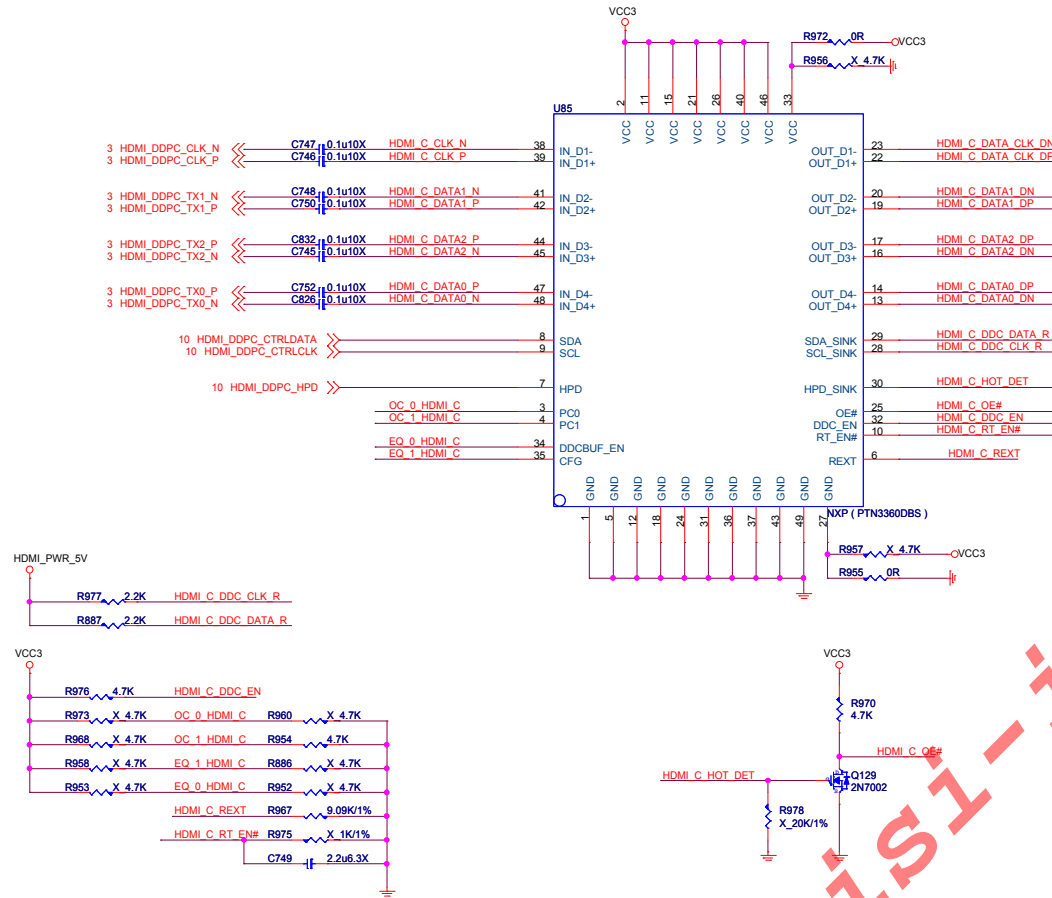
[DDC_EN, DDCBUF_EN, OE#]	DDC Passive Switch	DDC Active Buffer	PC1, PC0	note
1, 0, X	On	Off	00	8 dB
1, 1, 0	Off	On	01	4 dB
1, 1, 1	Off	Off	10	12 dB
0, X, X	Off	Off	11	0 dB

Table 8-1. PCH PCI Express Tx/RX - HDMI Signal Mappings

Port	Digital Display Interface Differential Pairs	HDMI Signals	PCH Digital Display Interface Pins
Port B	DDSP_B_TX0_DN	TMDSEB_DATA2+	DDPB_0N
	DDSP_B_TX0_DP	TMDSEB_DATA2-	DDPB_0P
	DDSP_B_TX1_DN	TMDSEB_DATA3+	DDPB_1N
	DDSP_B_TX1_DP	TMDSEB_DATA3-	DDPB_1P
	DDSP_B_TX2_DN	TMDSEB_DATA0+	DDPB_2N
	DDSP_B_TX2_DP	TMDSEB_DATA0-	DDPB_2P
	DDSP_B_TX3_DN	TMDSEB_CLK#	DDPB_3N
	DDSP_B_TX3_DP	TMDSEB_CLK	DDPB_3P
	DDPB_HPD	DDSP_B_HPD0	Hot plug detect used by HDMI Port B.
	SDVO_CTRLCLK	HDMI0_CTRL_CLK	HDMI DDC lines for Port B
	SDVO_CTRLDATA	HDMI0_CTRL_DATA	



HDMI level shifter



	"0"	"1"	note
DDC_EN	DDC level shifter disable	DDC level shifter enable	internal pull-up at ~500K ohm.
RT_EN#	Input 50 ohm termination resistor enable	the input termination ; resistors are set to high impedances	internal pull-down at ~500K ohm.
OE#	enable	the chip is power down and input termination resistors will be at high impedance.	internal pull-down at ~500K ohm.
HPD_SINK	disable	enable	internal pull-down at ~200K ohm; 5V tolerant.
DDCBUF_EN	For DDC level shifting configuration, please refer to Table.		internal pull-down at ~500K ohm.
REXT			analog current generation.

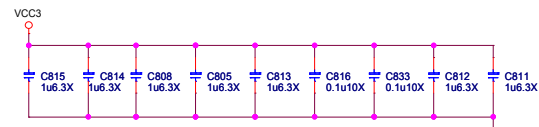
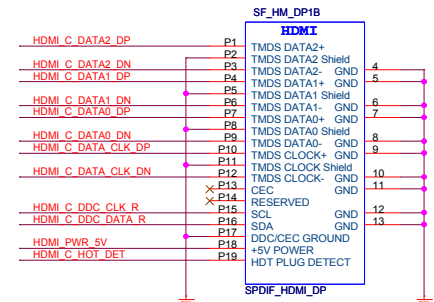
[DDC_EN, DDCBUF_EN, OE#]	DDC Passive Switch	DDC Active Buffer	PC1, PC0		note
1, 0, X	On	Off	00	8 dB	internal pull-down at ~500K ohm.
1, 1, 0	Off	On	01	4 dB	
1, 1, 1	Off	Off	10	12 dB	
0, X, X	Off	Off	11	0 dB	

EMI

HDMI_C_DATA_CLK_DN
HDMI_C_DATA_CLK_DP
HDMI_C_DATA1_DN
HDMI_C_DATA1_DP
HDMI_C_DATA2_DN
HDMI_C_DATA2_DP
HDMI_C_DATA0_DN
HDMI_C_DATA0_DP

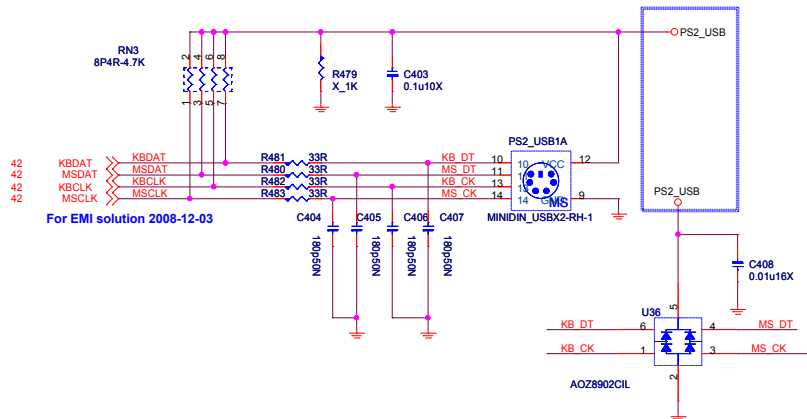
EMI cap.

HDMI_C_DDC_CLK_R C818 10p50N
HDMI_C_DDC_DATA_R C817 10p50N
HDMI_C_HOT_DET C803 10p50N



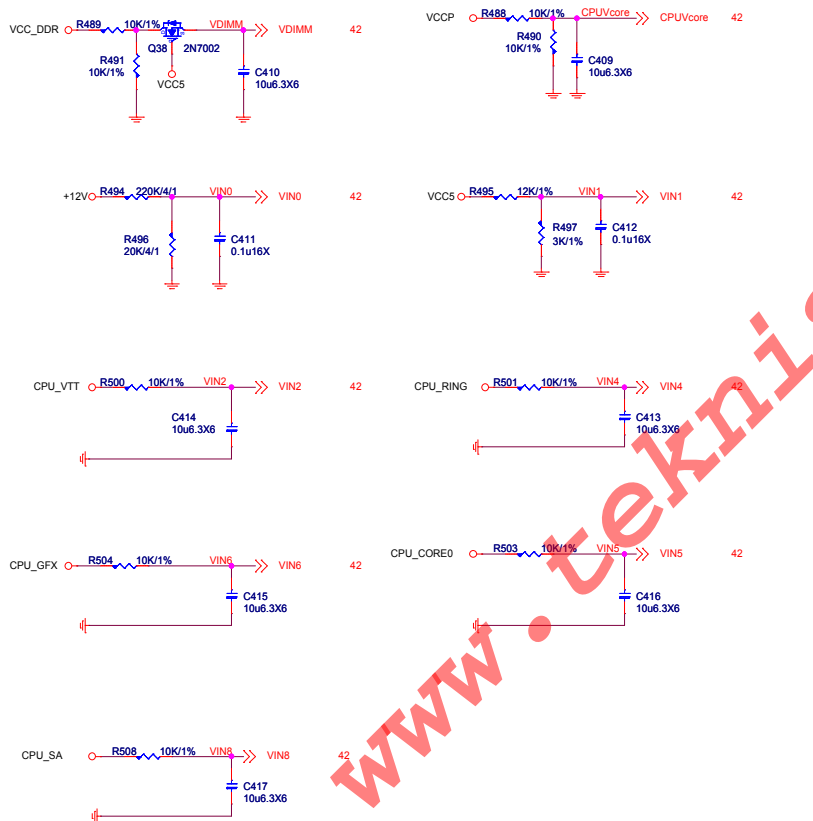
PS2 KEYBOARD & MOUSE CONNECTOR

可以切換在s5
底下是不是要有電

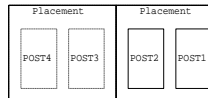


HW Monitor - Voltage

SIO HM Voltage voer 2V will not detect

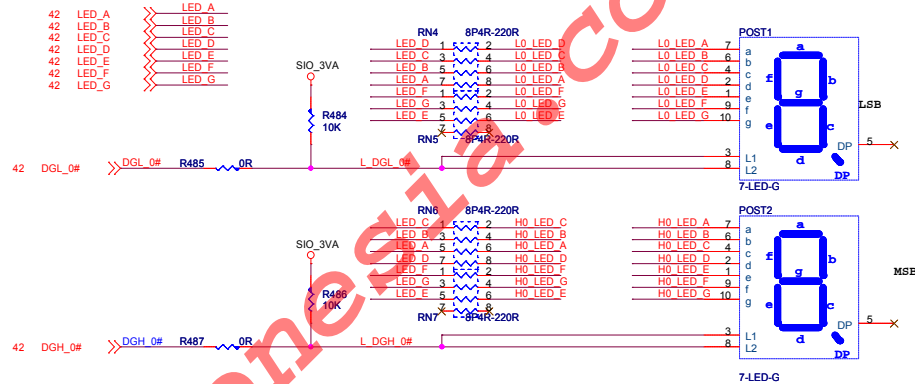


DEBUG LED

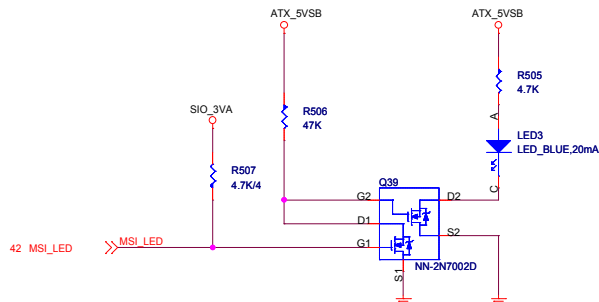


Placement一定要對

(DGH1=Post4/DGL1=Post3/DGH0=Post2/DGL0=Post1)



MSI_LED



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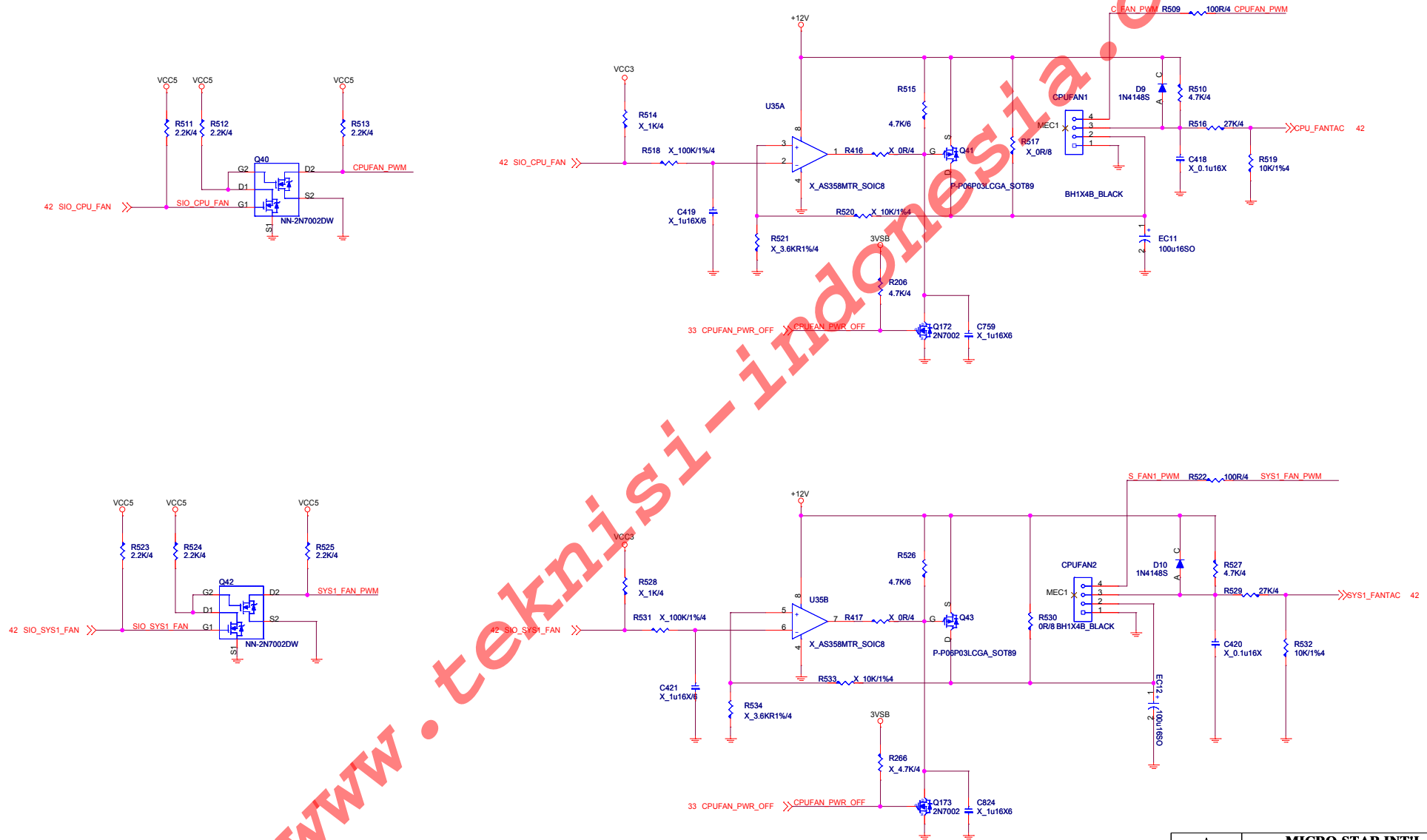
MS-7916

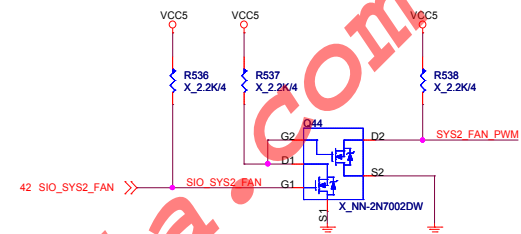
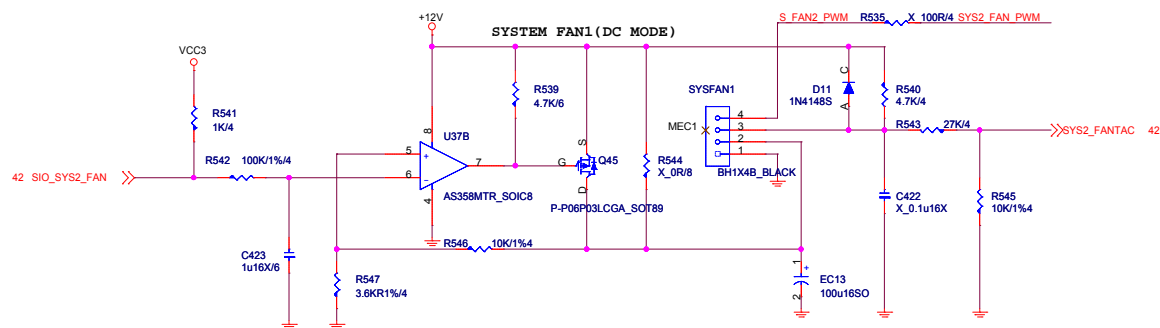
Size	Document Description
Custom	SIO-NCT6779D/PS2/Debug LE

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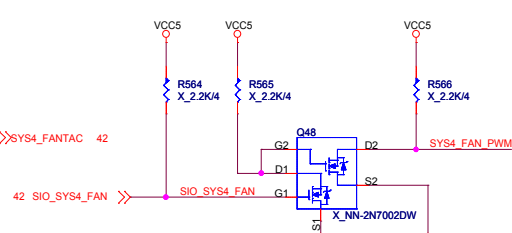
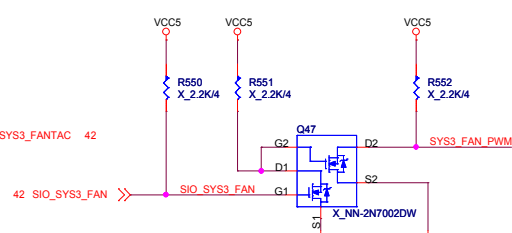
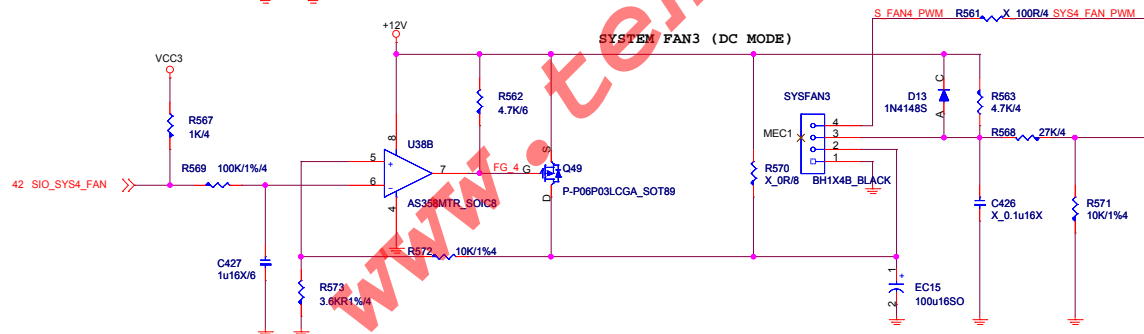
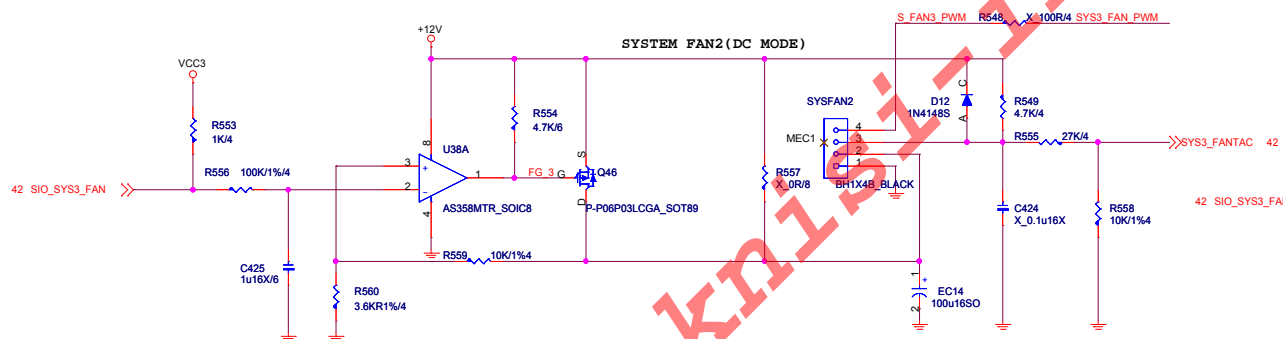
Type E : 4 PIN CPU FAN FROM SIO (Smart Fan/PWM MODE)(FOR NCT6776/5533)

CPUFAN





Type F : 4 PIN SYSTEM FAN FROM SIO (Smart Fan/PWM MODE)(FOR NCT6776/5533)

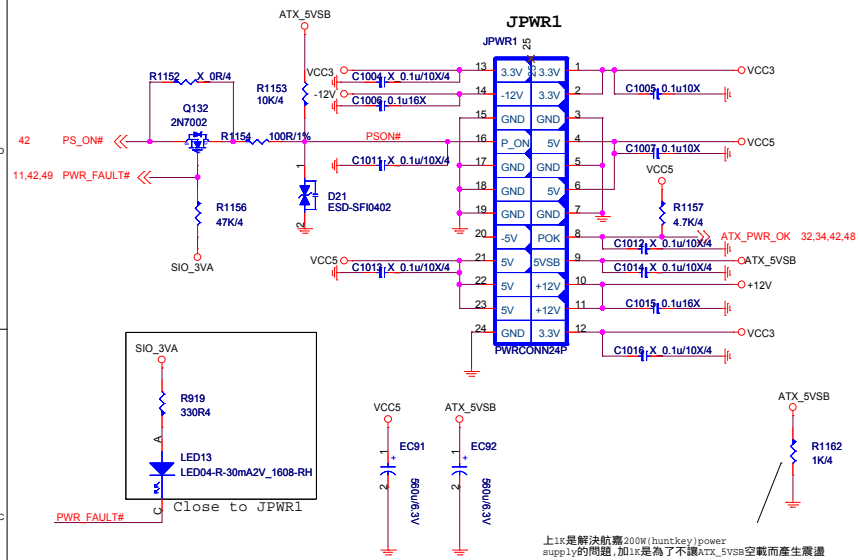


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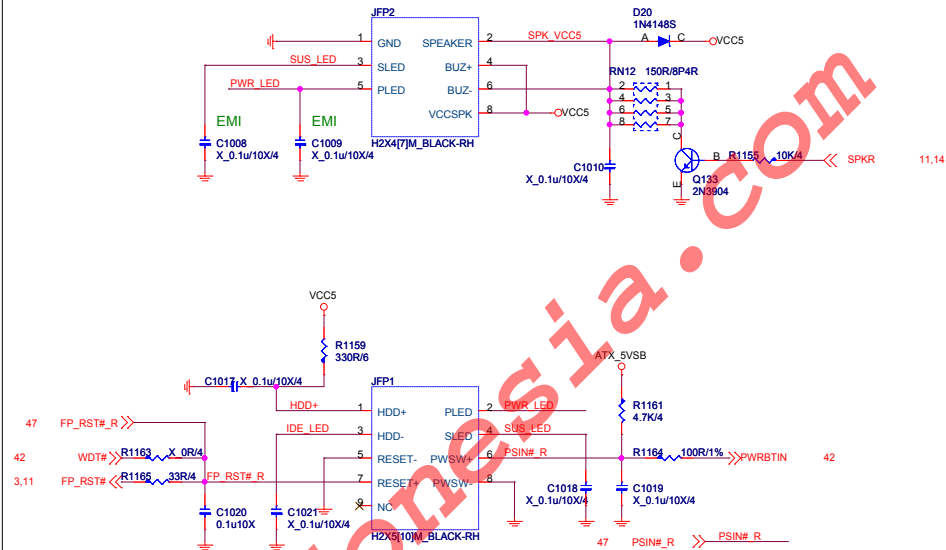
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		SYSFAN3-6	1.0
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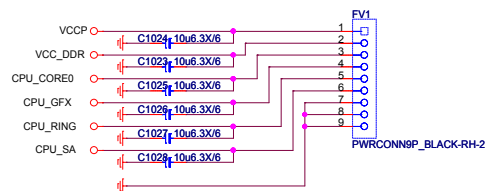
ATX POWER CONNECTOR



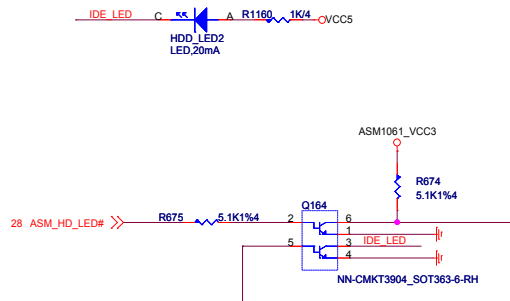
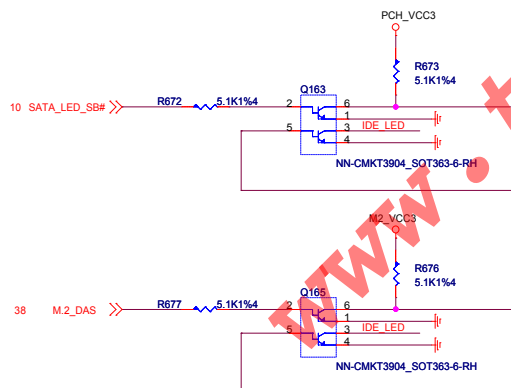
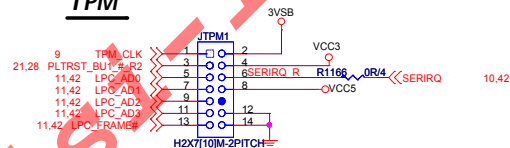
FRONT PANNEL



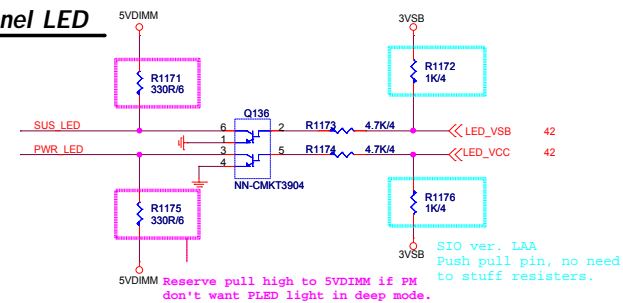
Voltage test point



TPM



Front Panel LED



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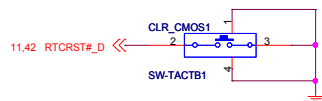
MS-7916

Size	Document Description
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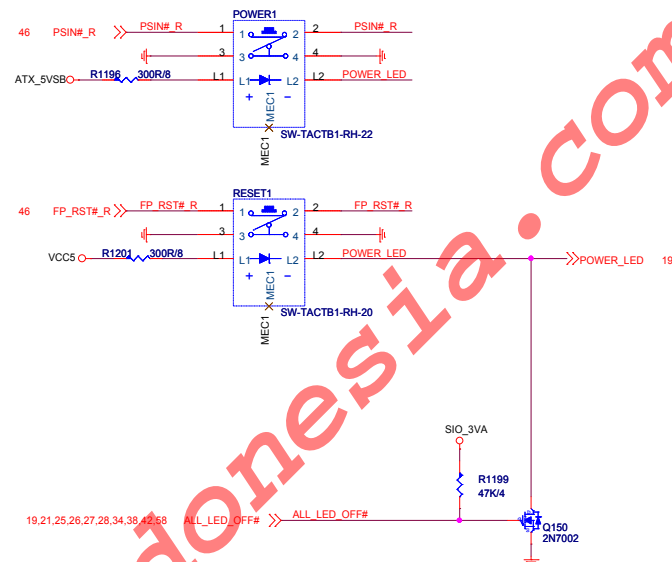
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Clear CMOS button

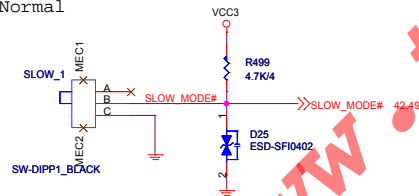


PWR/RST Button



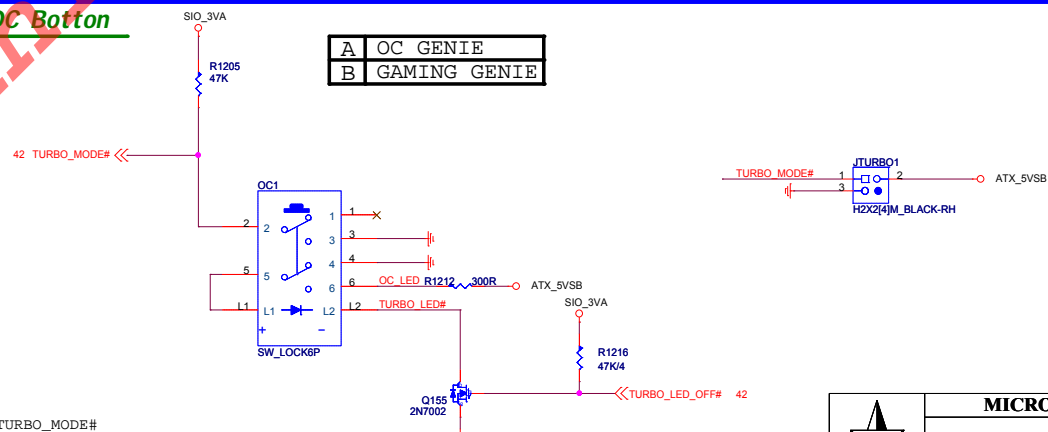
SLOW MODE

A Normal



B Slow Mode

OC Button



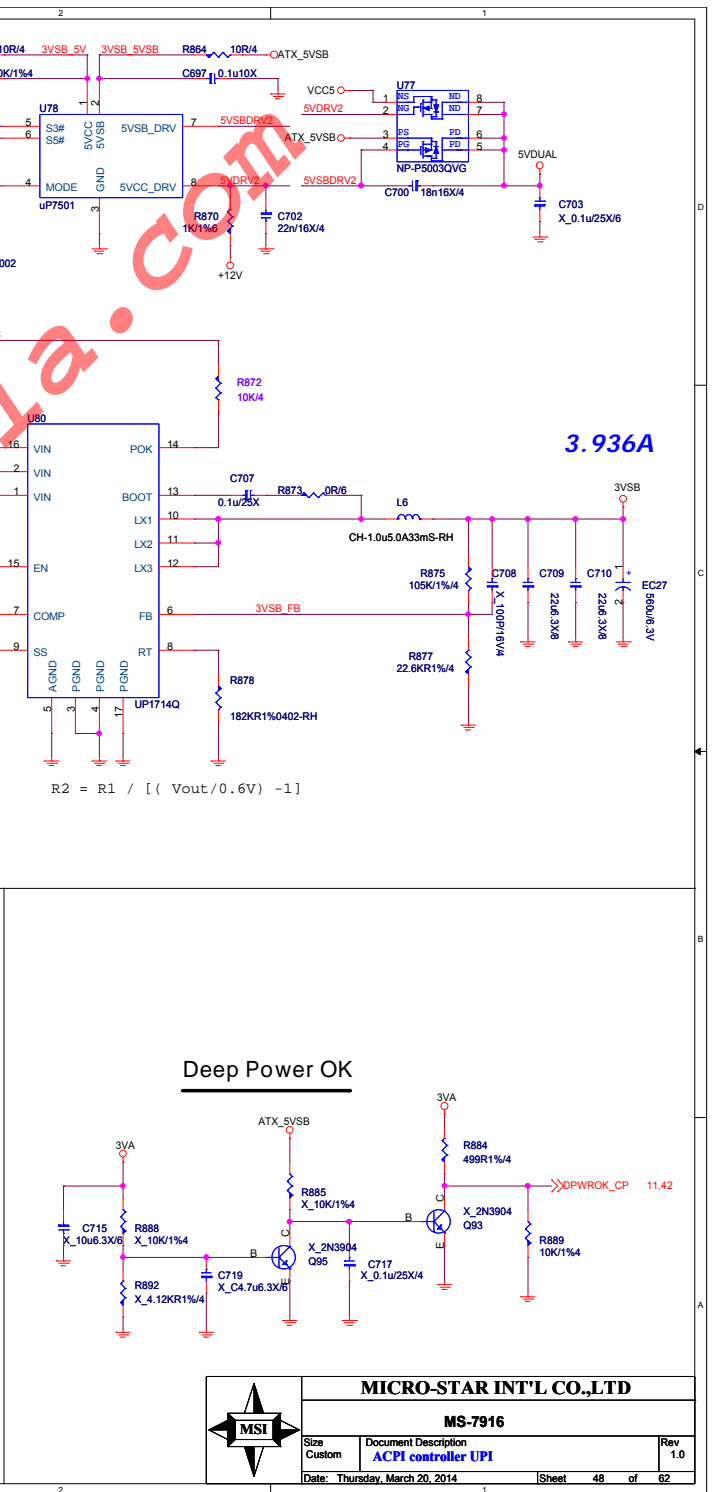
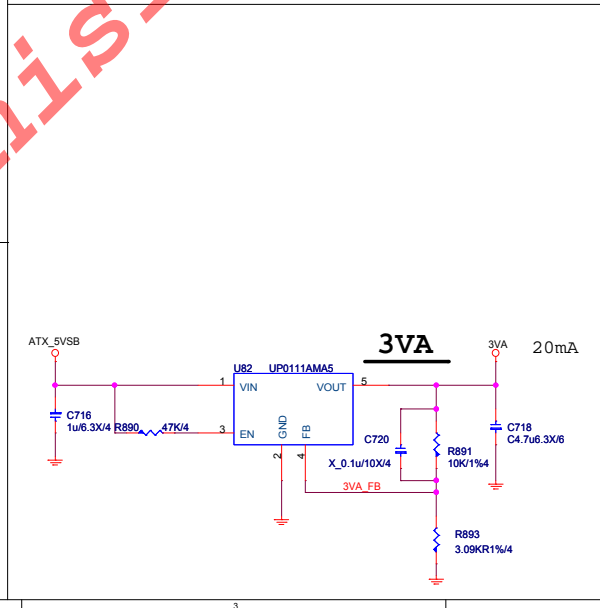
TURBO_MODE#
Default: Low,disable OC
Push Bottom: high,Enable OC / Turn on LED

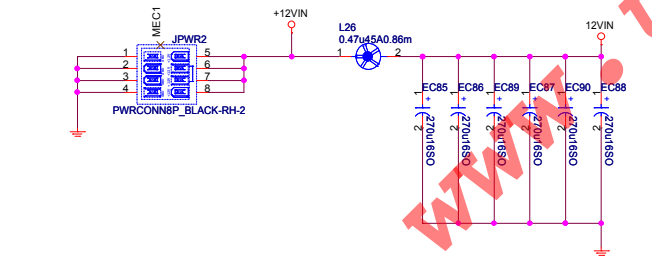
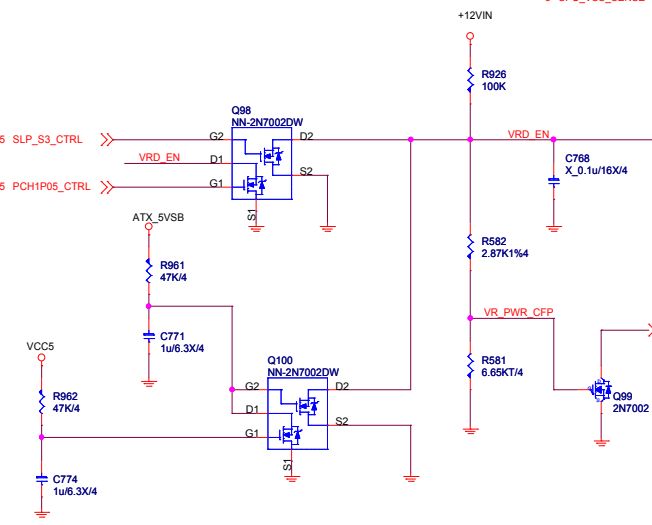


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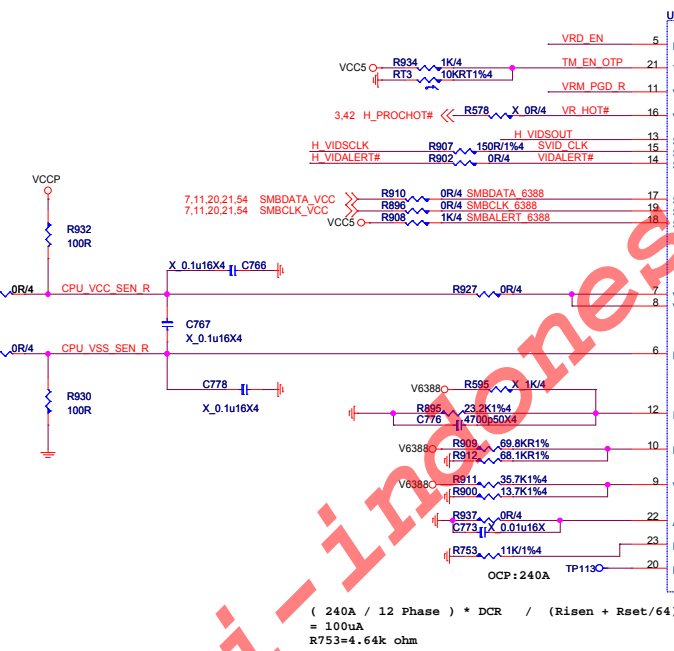
Size	Document Description	Rev
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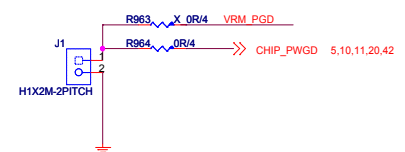
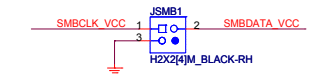
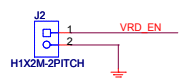
[illegible]

3 H_VIDALERT# <<< H_VIDALERT# R574 X 110R/1%
3 H_VIDSCLK >>> H_VIDSCLK R576 54.9R/1%
3 H_VIDSOUT <<< H_VIDSOUT R575 110R/1%

between 3 to 6 inches


$$\begin{aligned} & (240\text{A} / 12 \text{ Phase}) * \text{DCR} / (\text{Risen} + \text{Rset}/64) \\ & = 100\mu\text{A} \\ & \text{R753} = 4.64\text{k ohm} \end{aligned}$$


```
close phase sequence 6-3-5-2-4-1
address:8AH
```



ATX 5VSB

R951
47K/4

Q126

G2

D1

G1

D2

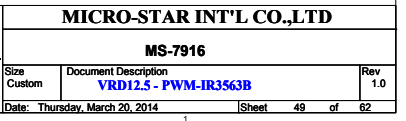
S2

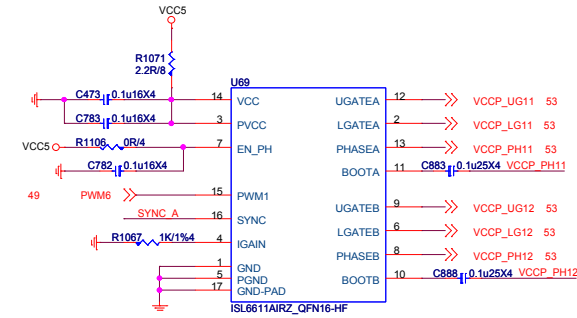
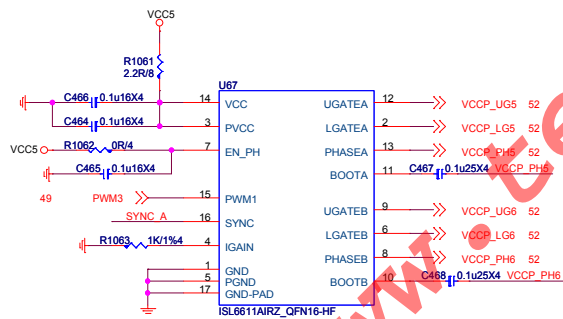
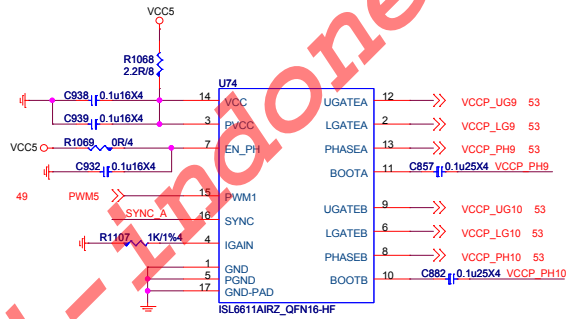
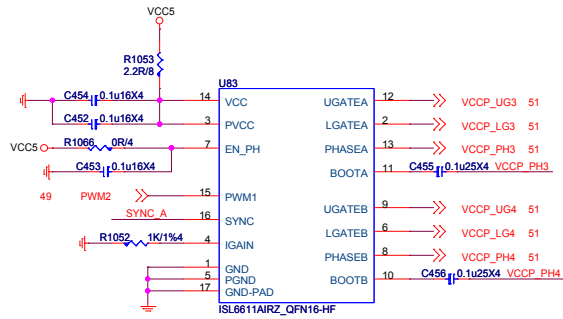
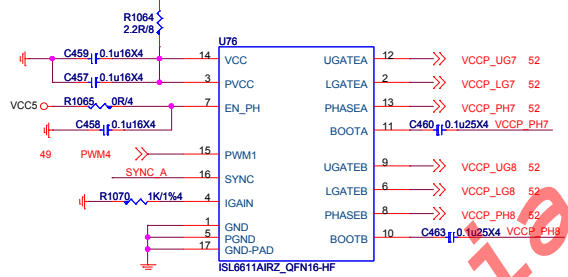
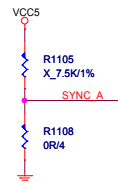
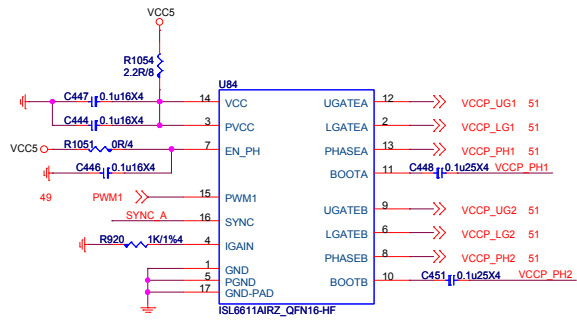
42.47 SLOW_MODE# >> SLOW_MODE#

H_PROCHOT# 3.42

NN-2N7002D

0

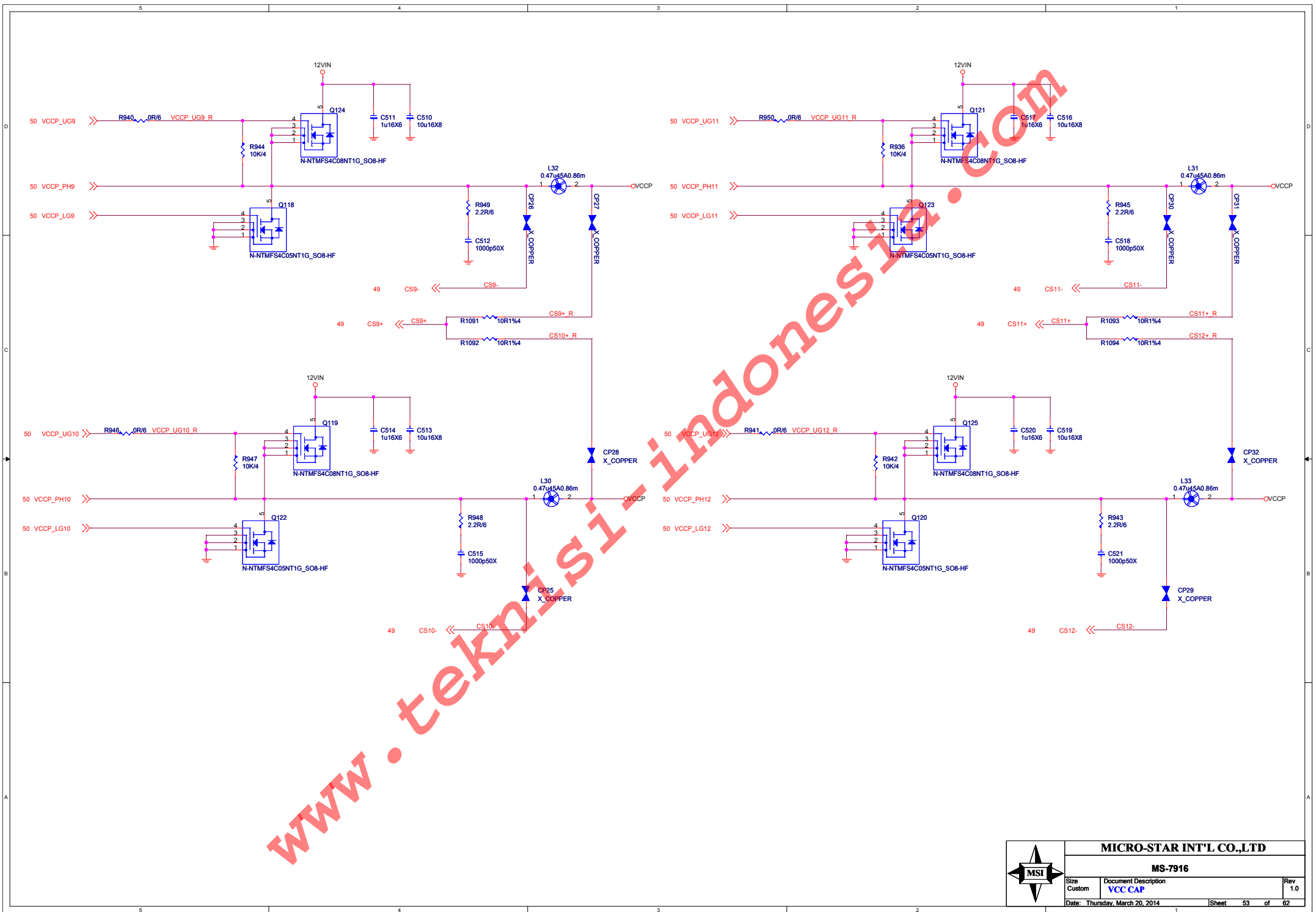




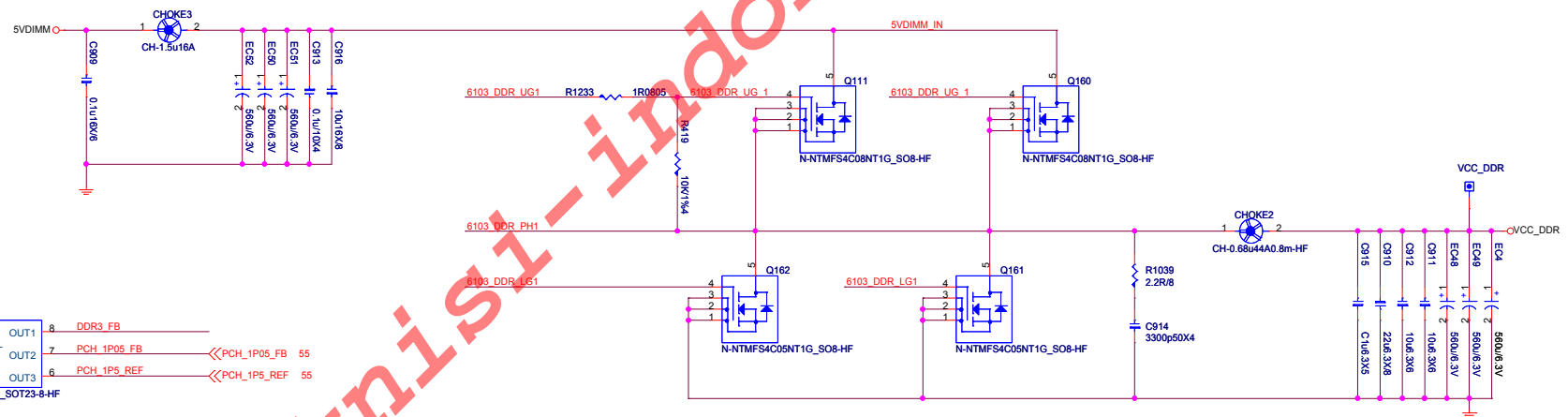
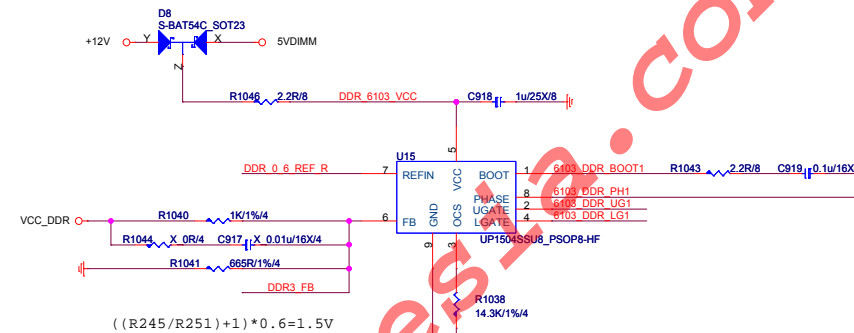
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MS-7916

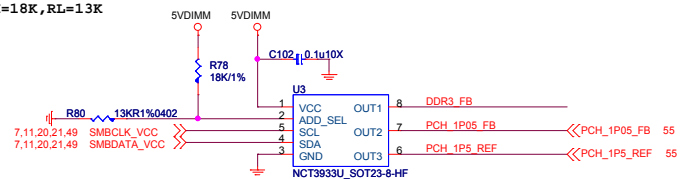
Size	Document Description	Rev
Custom	PHASE DOUBLER 3599 Phase1-16	1.0
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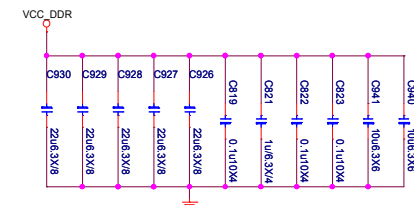
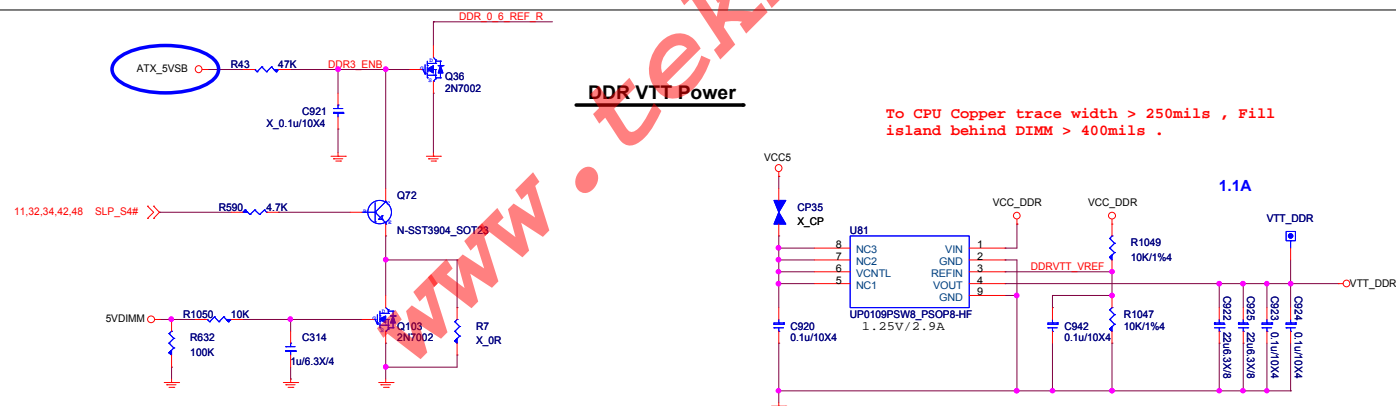
$R_{103}=14.3K\ ohm$



0x26:RH=18K,RL=13K



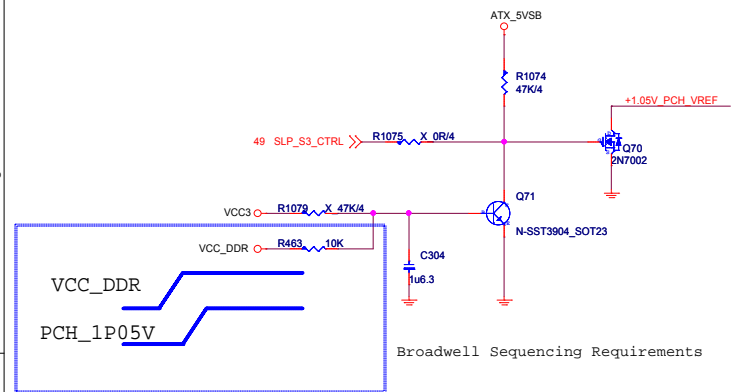
To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .



Size Custom	Document Description UP1504S DDR POWER	Rev 1.0
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PCH Power:1.05V

6A

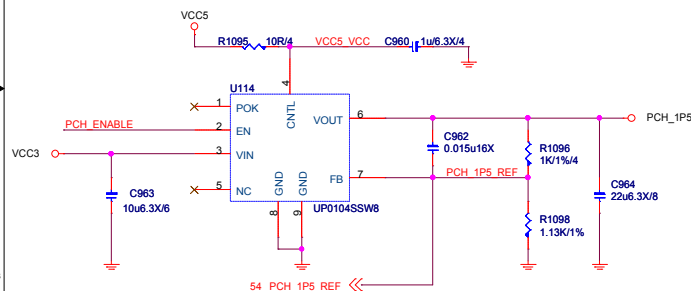
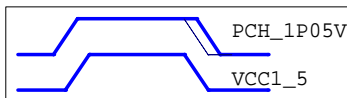


VCC1_5_CTRL_INPUT:
0:1P05V low or S3 low
1:1P05V HIGH and S3 HIGH

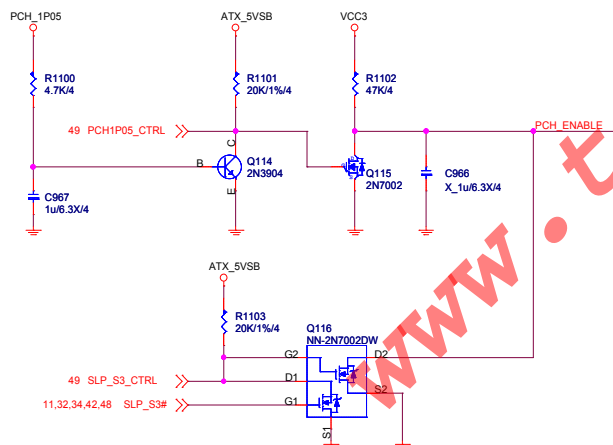
PCH_1P5

PCH: 0.35A

OV: 一階10mV



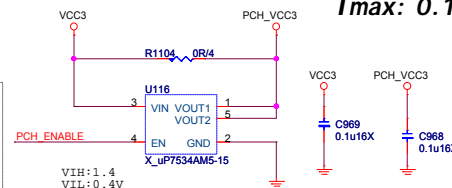
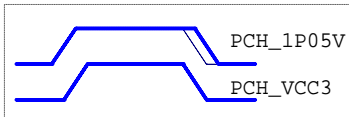
Waiting PCH_1P05 Ready



VCC1_5_CTRL_INPUT:
0:1P05V low or S3 low
1:1P05V HIGH and S3 HIGH

PCH_VCC3

I_{max}: 0.133A



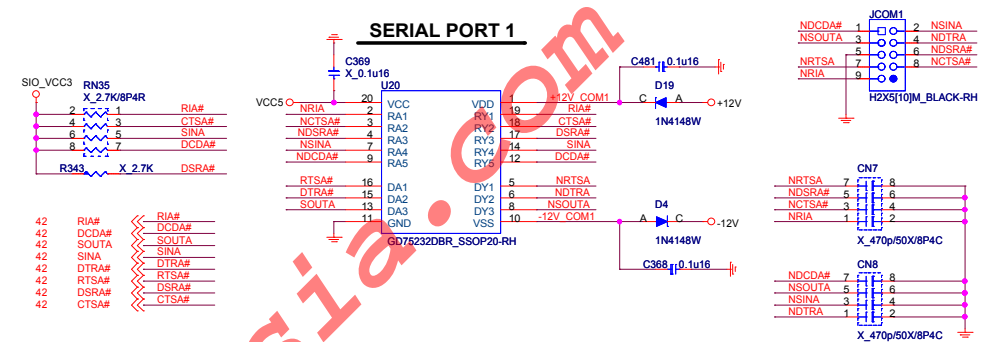
MICRO-STAR INT'L CO.,LTD

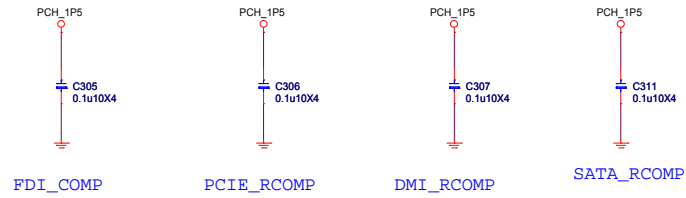
MS-7916

Size	Document Description	Rev
Custom	LYNX Power -PV3101	1.0

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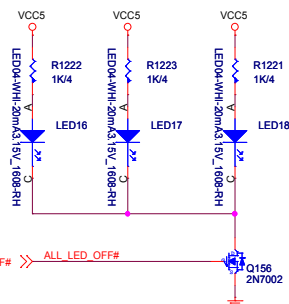
www.teknisi-indonesia.com





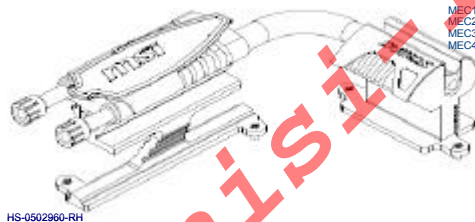
www.teknisi-indonesia.com

PCH



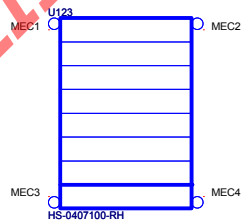
CPU Sink 料號

U122



HS-0502960-RH

PCH Sink 料號



HDMI Label Part Number



HDMI Virtual Part Number



X_BIOS LABEL



CPU_H1



SLI LABEL



Creative



X_MB3



X_Virtu Universal MVP LABEL



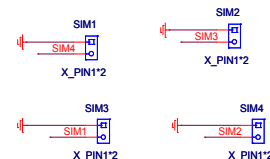
7916_0A



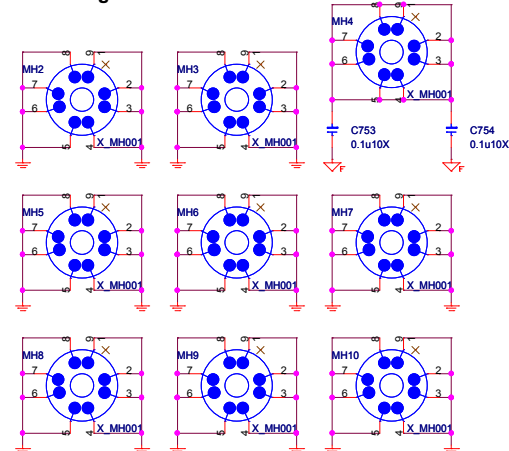
BAT-BCR2032P-RH

PD0-0791610-G37, 精成, 23, 寶安恩斯邁廠 (MSIS)
PD0-0791610-E48, 競華, 23, 寶安恩斯邁廠 (MSIS)

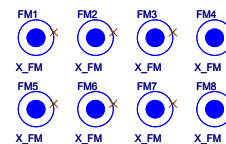
Simulation



Mounting Holes



Optical Fiducial Marks-120



OPT	Configure	BOM	Function
		601-7751-10S	MS-7751 30 Z77 MPower 4*DDR3+3*PCI-Ex16,4*PCI-Ex1,+4*SATAII+2*SATAIII +8*USB2.0+8*USB3.0+HD 8Ch Audio+HDMI+DisplayPort+Gb LAN,Hi-C CAP,EuP,RoHS

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MS-7916			
Size Custom	Document Description Manual Parts	Rev 1.0	
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